Study of Leakage Power, Controlled by Input Vector Technique

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Abstract: In the scaling of MOS devices requires use of ultra-thin gate oxides to maintain a reasonable short channel effect. Such thin oxides give rise to high electric fields, resulting in considerable direct tunneling current. For CMOS devices with thicker oxides, the major leakage mechanism is sub-threshold current, which increases due to the short channel effect. Hence, circuit techniques used to control sub-threshold leakage need to be reinvestigated to evaluate their effectiveness in improving the overall leakage current. The "transistor stacking" technique is proven to be extremely effective in lowering sub-threshold leakage in the standby-mode of operation of a circuit. This paper presents to determine the input vector that minimizes leakage current of nanometer CMOS circuits during sleep mode considering stack effect.
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1. Introduction

Due to the continued scaling of technology and supply/threshold voltage, leakage power has become more and more significant in power dissipation of nano-scale CMOS circuits. Therefore, the estimation of the total leakage power is critical to design low power digital circuits.

In nanometer CMOS circuits, the main leakage components are sub-threshold, gate tunneling, and reverse biased junction band-to-band-tunneling (BTBT) leakage current. As transistor geometries are reduced, it is necessary to reduce the supply voltage to avoid electrical break down and to obtain the required performance. However, to retain or improve performance it is necessary to reduce the threshold voltage as well, which results in exponential increase of sub-threshold leakage. To control short channel effect and increase the transistor driving strength in deep sub-micron (DSM) circuits, gate-oxide thickness also becomes thinner as technology scales down [1].

The aggressive scaling in the gate-oxide results in tunneling current through the oxide, which is a strong exponential function of the oxide thickness and the voltage magnitude across the oxide. In scaled devices, the higher substrate doping density and the application of the "halo" profiles cause significantly large reverse biased junction band-to-band-tunneling (BTBT) leakage current through drain-substrate and source-substrate junctions. This problem is very serious in portable electronic systems that operate mostly in sleep mode. In order to minimize the leakage power dissipation, several circuit techniques have been proposed such as multi-threshold voltage CMOS (MTCMOS) using sleep transistor, variable threshold voltage CMOS (VTCMOS) using variable substrate bias voltage. However, these techniques require significant circuit modification and performance overhead for leakage reduction. Another technique with little or no overhead is the input pattern control technique based on stack effect: the amount of leakage currents of nanometer CMOS circuit varies depending on the input pattern [7]. However, it is hard to determine the input pattern that sets up the minimum leakage current during standby mode without any hardware overhead or architecture change. Several techniques have been proposed to generate the minimum leakage test pattern and solve the problem. None of these techniques explicitly considers the interactions between the sub-threshold leakage and gate tunneling leakage, body effect and fan-out effect. Therefore, better understanding and more accurate model of leakage currents are required for the input pattern control in the nanometer CMOS circuits.

Figure (1) and Figure (2) show the leakage current in nano-scale CMOS circuit. Figure (1) show the leakage current when transistor is in off state means their gate to source voltage is zero. Figure (2) show the leakage current mechanism when the transistor is in on or active mode [2].

2. Experimental Results and Discussion

Sub-threshold leakage current flowing through a stack of series-connected transistors reduces when more than one transistor in the stack is turned off. This effect is known as the stacking effect. When there are two or more stacked off-transistors, the sub-threshold leakage is reduced. This reduction depends on the choice of the input pattern during standby periods because it determines the number of off transistor in the

stack. Turning off more than one transistor in a stack of transistors forces the intermediate node voltage to go to a value higher than zero. This causes a negative Vgs, negative Vbs (more body effect) and Vds reduction (less DIBL) in the top transistor, thereby reducing the sub-threshold leakage current flowing through the stack considerably, which is known as the stack effect. When NMOS transistors are used, then it is called forced NMOS stacking [3-4].

Stacking of two devices that are off has significantly reduced leakage compared to a single off device. Figure (4) show the result of leakage current and no. of transistors are connected in the stack. If no. of transistors are more in stack this cause less leakage current flow, it is due to increase the intermediate node voltage and hence body to substrate voltage. Figure (3) show the leakage current variation due to variation in body voltage at different supply voltage.

However due to the iso-input load requirement and due to stacking of devices, the drive current of a forced-stack gate will be lower resulting in increased delay. So, stack forcing can be used only for paths that are non-critical, just like using high-*Vt* devices in a dual-*Vt* design. Forced-stack gates will have slower output edge rate similar to gates with high-*Vt* devices.
By properly employing forced-stack one can reduce standby and active leakage of non-critical paths even if a dual-*Vt* process is not available. This method can also be used in conjunction with dual-*Vt*. Stack forcing provides wider coverage in the delay leakage trade-off. By maximizing the number of natural stacks in off state during standby by setting proper input vectors, the standby leakage of functional block can be reduced. Since it is not possible to force all natural stacks in the functional block to be in off state the overall leakage reduction at a block level will be far less than the stack effect leakage reduction possible at a single logic gate level. With stack forcing the potential for leakage reduction will be higher [5].

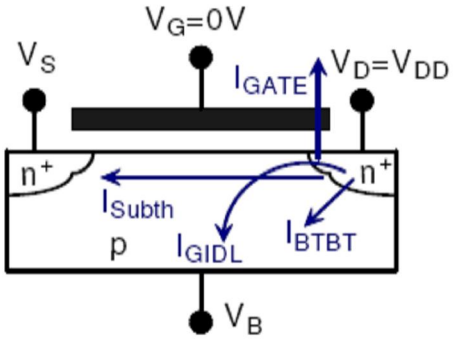

Figure (1) Off-State Leakage Components in Nano-scale CMOS Circuit

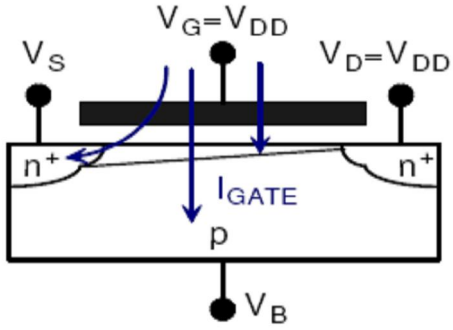

Figure (2) On-State Leakage Components in Nano-scale CMOS Circuit

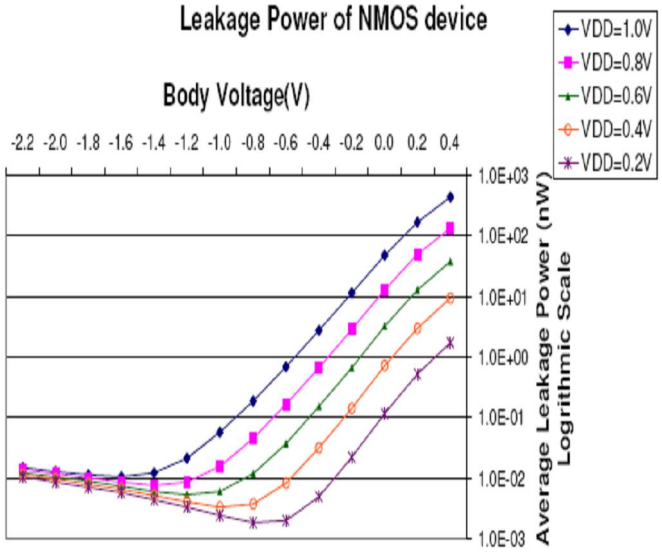

Figure (3)

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Input A	Input B	Input C	Leakage Current (nA)
0	0	0	0.91
0	0	1	1.86
0	1	0	1.86
0	1	1	17.59
1	0	0	1.78
1	0	1	11.89
1	1	0	10.98
1	1	1	91.87

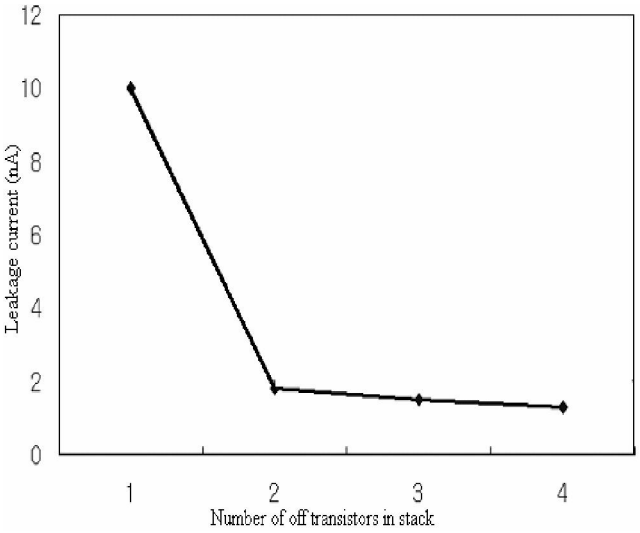

Figure (4)

Forcing a stack in both n- and p-networks of a gate will guarantee leakage reduction due to stacking, independent of the input logic level. Gates that can force stack effect independent of its input vectors will automatically go into leakage reduction mode when the intermediate node of the stack reaches the steady state voltage. This will boost standby and active leakage reduction since no specific input vector needs to be applied.

Figure (4) gives the leakage current trends of each stacked transistors as a function of transistor number. The leakage current decreases monotonously with the number of stacked transistors.

Because of the transistor stack effect, the leakage current of a gate depends on its input combination. Individual CMOS gates show a variation in the leakage power based on different input patterns. As shown in Figure (5) 3-input NAND gate, only a few of input patterns have significant leakage, and they are defined as ”Dominant Leakage States” which has only one transistor off in the path from Vdd to Gnd node. Therefore, ”011”, ”101”, ”110”, and ”111” input patterns of 3-input NAND gate are dominant leakages states [7].

Table (1) show the leakage current, result of this 3-input NAND gate for different input combinations. For input combination ‘000’ minimum leakage current occur. Input combination 000 the all three transistors in pull down network are in off condition, this cause the intermediate node voltage incremented and hence decremented in leakage current. Maximum leakage current occurs for input combination ‘111’, because all three transistors in pull down network are in on state, this cause decrease in intermediate node voltage and hence more leakage current.

Table (1) Leakage Current with different inputs

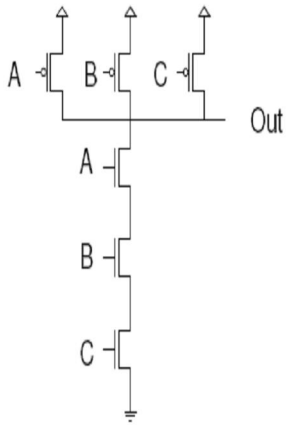

Figure (5)

Conclusion

We could see that in deep submicron processes leakage consumption is playing a more and more important role in the total power consumption and more and more research both from academic and industry are being conducted in this area. Methods like input vector control are limited by the controllability of internal nodes and thus may be difficult for complex circuits. The effectiveness of this technique will depend on specific application and it themselves still need to be matured. But reducing leakage consumption is becoming more and more important. So we can predict that there will be more research in this and other techniques like multi threshold, variable threshold, dual threshold and they will need to be reevaluated in each process generation since the changing leakage mechanisms will dictate the effectiveness of these techniques.

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References

Journals:

1. Siva G. Narendra, Anantha Chandrakasan, "Leakage in Nanometer CMOS Technologies (Series on Integrated Circuits and Systems)", Springer, Nov. 2005.
2. Feng Gao, John P. Hayes, "Exact and Heuristic Approaches to Input Vector Control for Leakage Power Reduction, Computer Aided Design", ICCAD-2004, Page(s)527-532, Nov. 2004.
3. Rahul Kumar, C.P. Ravikumar, "Leakage power estimation for deep submicron circuits in an ASIC design environment", International conference on VLSI Design(VLSID'02), Page(s)45-50, Jan. 2002.
4. M. Powell, S.-H. Yang, B. Falsafi, K. Roy and T. N. Vijaykumar, "Gated-Vdd: A Circuit Technique to Reduce Leakage in Deep submicron Cache Memories," International Symposium on Low Power Electronics and Design, pp. 90-95, July 2000.
5. Z. Chen, M. Johnson, L. Wei and K. Roy, "Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistor Stacks," International Symposium on Low Power Electronics and Design, pp. 239-244, August 1998.

Proceedings:

6. Yongjun Xu, Zuqing Luo, "Minimum leakage Pattern Generation Using Stack Effect", In proceeding of ASICON'03,Page(s)1239-1242, Oct. 2003
7. J.C. Park, V. J. Mooney and P. Piffenberger, "Sleepy Stack Reduction of Leakage Power," Proceeding of the International Workshop on Power and Timing Modeling, Optimization and Simulation, pp. 148-158, September 2004.

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