Double-gate LDMOSFET High-voltage Devices for Medium Voltage Applications

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Abstract: A one-dimensional compact model of a double-gate LDMOSFET is presented in this work. The impact of controlling the drift region resistance by controlling the bias and/or gate metal work function of a separately added second gate of the LDMOSFET electrostatics is investigated. Compact models for the charges and currents are introduced. The effect of the second gate on the current-voltage characteristics and different capacitances, are studied in this work. Numerical simulation emphasized the effect of second gate bias on current-voltage characteristics and showed its effect on capacitances. The results of the study show that by controlling bias of the second gate, DC and AC characteristics pronounced as current and capacitances can be altered to obtain an optimized device performance based on requirement.
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1. Introduction

High-voltage transistors are drawing attention nowadays as there is a need to optimize the usage of energy to reduce switching losses. It is important to develop a device that can accommodate high voltages for use in suitable targeted applications [1-4]. A tradeoff between on-resistance and breakdown voltage shall be made according to device application. The bulk LDMOSFET is a good candidate its low manufacturing cost. Many research efforts have investigated LDMOSFET from different perspectives, with the device having either one gate extended over the entire distance from the source to the drain [5], a partial overlap of the drift region [6-8], or having a double-gate device with an extra added separately-biased gate [9].

Some Studies have examined the current-voltage characteristics and how they are affected by different drift region parameters, such as the drift region length, device width, and drift region doping level, which are all related to the drift region resistance. Drift region resistance affects the breakdown behavior of the LDMOSFET high-voltage device. Drift region resistance and breakdown voltage need to be traded off for achieving specific application target of LDMOSFET devices. It might be simply thought off as when doping concentration of drift region is increased more carriers will exist so drift region conductivity will increase. However, potential of the internal drain point for the intrinsic MOSFET part will increase, which will make it more vulnerable to breakdown and reduce the entire device breakdown voltage. Also, when increasing the drift region length, this will cause the drift resistance to decrease which in-turn causes the breakdown voltage to increase. This tradeoff between the drift region resistance and breakdown voltage can be calculated using equation [1],

$$R_{on-ideal} = \frac{4\,BV^2}{\epsilon_s \mu_n E_c^3} \qquad (1)$$

Where, BV is the breakdown voltage, ϵ_s is the silicon permittivity, μ_n is the electron mobility, and E_c is the critical electric field for silicon. Other studies have proposed modifications of the LDMOSFET structure to decrease the drift region resistance [9-11].

In this paper, a more investigative study of double-gate LDMOSFET is done. Emphasis of the effect of a separately biased second gate is done. This second added gate covers the entire drift region starting from the intrinsic MOSFET drain point (internal drain) to the drain of the LDMOSFET device.

The second separately biased gate that is added above the drift region provides more degree of freedom controlling on-resistance in a dynamic way without changing process parameters.

A two-dimensional model has been developed earlier for the same structure which focused on surface potential, electric field, and short channel effects [10].

In this work, a 1-D compact model is introduced which includes both the intrinsic MOSFET and drift region parts. The effect of the bias of the second gate is emphasized by studying its effect on the DC characteristics and AC characteristics. Model for current-voltage characteristics has been developed. 2D simulator results for current-voltage characteristics confirmed the effect of the bias of the second gate and

effect of the bias of the second gate is studied to on different capacitances as well.

The remainder of this work is organized as follows: The 1D charges and current model is presented in section II, the 2D simulator results of current-voltage characteristics and capacitances are presented in section III. Finally conclusion and remarks is presented in section IV.

All of the calculations in this work are performed at room temperature. Additionally, the parameters are presented in Table I. It important to note here that those values presented on Table I below do not represent real technology parameters value; they are arbitrary values used for our study and it is not meant to be best optimized for real devices.

Table I: Device Parameters

Parameter	Value	Unit
Gate oxide thickness, t_{ox}	38	nm
Bulk doping concentration, N_A	$3 * 10^{17}$	cm^{-3}
Drift region doping concentration, N_D	$5 * 10^{16}$	cm^{-3}
Gate 1 length, L_1	1	µm
Gate 2 length, L_2	1	µm
Source and drain ohmic contact doping concentrations, N_d	10^{21}	cm^{-3}
Bulk region depth, d_1	1	µm
Drift region depth, d_2	2	µm

1-D Model Analysis For The Charges And Current

Figure 1 shows a cross section of the double-gate LDMOSFET (DG-LDMOS) with two gates that have lengths of L_1 and L_2. There should be an insulation barrier between both gates to separately bias them. This barrier is neglected for simplicity and is not shown in the figure. The DG-LDMOS device is divided into two regions, the intrinsic MOSFET region (region I) and drift region (region II). Region I is p-type whereas region II is a lightly doped n-type. From Fig. 1, the DG-LDMOS device can be constructed using a double-diffusion process where the bulk (p-type) of the intrinsic MOSFET part (region I) can be fabricated by diffusing holes from the left side (source side) [7], which means that the bulk of region I is non-uniformly doped. The effect of the non-uniform doping of region I was not considered here. However, some other research efforts addressed this issue for the standard bulk LDMOSFET [7]. In Fig. 1, both gates of the DG-LDMOS may have different work functions or have different biases applied to have more separate flexible control [10].

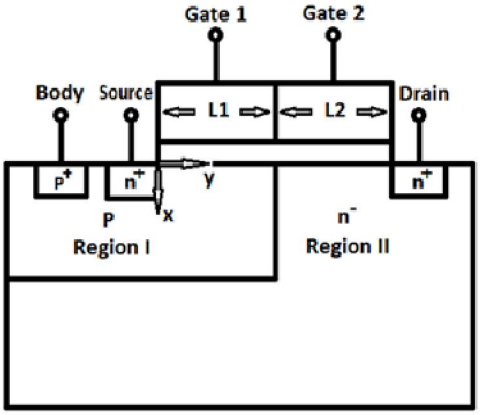

Figure 1. Cross section view of the introduced double-gate LDMOSFET (DG-LDMOS).

$$\mathbf{Q_G = C_{ox}\,\varphi_{ox}} \quad (2)$$

$$\mathbf{Q_B = -\sqrt{2\,q\,\in_s N_A}\,\sqrt{\varphi_s}} \quad (3)$$

$$\mathbf{Q_I = -Q_G - Q_B} \quad (4)$$

$$\mathbf{Q_I(\varphi_s) = -C_{ox}\,(V_{GB} - \varphi_s - \emptyset_{ms}) + \sqrt{2\,q\,\in_s N_A}\,\sqrt{\varphi_s}} \quad (5)$$

For Region I (Intrinsic MOSFET part):

At the source, $\boldsymbol{\varphi_s = \varphi_{s0}}$ and at the drain, $\boldsymbol{\varphi_s = \varphi_{sL1}}$

The current is due to two components, drift component due to electric field and diffusion component due to interaction with carriers (electrons in this case) with p-n junction at the source-channel and drain-channel junctions.

Then,

$$\mathbf{I_D = I_{Ddrift} + I_{ddiff}} \quad (6)$$

$$\mathbf{I_{D1} = \frac{W}{L_1}\int_{\varphi_{s0}}^{\varphi_{sL1}} \mu\,(-Q_I(\varphi_s))\,d\varphi_s + \frac{W}{L_1}\,\emptyset_t\int_{Q_{I0}}^{Q_{IL1}} \mu\;dQ_I} \quad (7)$$

The above equation is showing that the drift component of current in the channel of region I is due to mobile carriers (inversion charges) and surface potential difference between source and internal drain who are swept toward drain through the internal drain point Di. Also it shows that the diffusion component of current is due to gradient of charges between source and internal drain points.

Substituting from equation (5) in (7) and applying integration, the channel current or region I current $\mathbf{I_{D1}}$ is given by:

$$\mathbf{I_{D1}} = \frac{\mathbf{W}}{\mathbf{L_1}}\,\boldsymbol{\mu}\,\mathbf{C_{ox}}\{(\mathbf{V_{GB}} - \boldsymbol{\emptyset_{ms1}})(\boldsymbol{\varphi_{sL1}} - \boldsymbol{\varphi_{s0}}) - \mathbf{0.5}\left(\boldsymbol{\varphi_{sL1}^2} - \boldsymbol{\varphi_{s0}^2}\right) - \mathbf{0.67}\,\boldsymbol{\gamma_1}\left(\boldsymbol{\varphi_{sL1}^{1.5}} - \boldsymbol{\varphi_{s0}^{1.5}}\right) + \boldsymbol{\emptyset_t}(\boldsymbol{\varphi_{sL1}} - \boldsymbol{\varphi_{s0}}) + \boldsymbol{\emptyset_t}\,\boldsymbol{\gamma_1}\left(\boldsymbol{\varphi_{sL1}^{0.5}} - \boldsymbol{\varphi_{s0}^{0.5}}\right)\} \quad (8)$$

In order to get $\boldsymbol{\varphi_{sL1}}$ and $\boldsymbol{\varphi_{s0}}$,

$$\mathbf{V_{GB}} = \boldsymbol{\emptyset_{ms}} + \boldsymbol{\varphi_s} - \frac{\mathbf{Q_S}}{\mathbf{C_{ox}}} \quad (9)$$

$$\mathbf{Q_S} = -\mathbf{Q_G} = \mathbf{Q_B} + \mathbf{Q_I} \quad (10)$$

$$\mathbf{V_{GB}} = \boldsymbol{\emptyset_{ms}} + \boldsymbol{\varphi_s} + \boldsymbol{\gamma}\sqrt{\boldsymbol{\varphi_s} + \boldsymbol{\emptyset_t} + \mathbf{e}^{(\varphi_s - 2\,\varphi_f - V_{SB})/\emptyset_t}} \quad (11)$$

Then,

$$\boldsymbol{\varphi_{s0}} = \mathbf{V_{GB1}} - \boldsymbol{\emptyset_{ms1}} - \boldsymbol{\gamma_1}\sqrt{\boldsymbol{\varphi_{s0}} + \boldsymbol{\emptyset_t} + \mathbf{e}^{(\varphi_{s0} - 2\,\varphi_f - V_{SB})/\emptyset_t}} \quad (12)$$

$$\boldsymbol{\varphi_{sL1}} = \mathbf{V_{GB1}} - \boldsymbol{\emptyset_{ms1}} - \boldsymbol{\gamma_1}\sqrt{\boldsymbol{\varphi_{sL1}} + \boldsymbol{\emptyset_t} + \mathbf{e}^{(\varphi_{sL1} - 2\,\varphi_f - V_{DiB})/\emptyset_t}} \quad (13)$$

Normally in the case of MOSFET, each of equations (12) and (13) are solved iteratively to obtain $\boldsymbol{\varphi_{s0}}$ and $\boldsymbol{\varphi_{sL1}}$ by setting $\mathbf{V_{Di}} = \mathbf{V_D}$.

In our case the channel current $\mathbf{I_{D1}}$ will be left in terms of $\boldsymbol{\varphi_{sL1}}$ and the value of $\boldsymbol{\varphi_{s0}}$ will be obtained iteratively through equation (12).

Therefore;

$$\mathbf{I_{D1}} = \mathbf{I_{D1}}(\boldsymbol{\varphi_{sL1}}) = \mathbf{I_{D1}}(\mathbf{V_{Di}}) \quad (14)$$

Equation (14) accounts for the channel current in the linear region. In order to get the current in saturation, this equation is differentiated with respect to $\mathbf{V_{Di}}$ and then the differentiation is set to zero and then the resulting equation is solved for $\mathbf{V_{Di}(sat)}$. Then a smoothing function is used to have the current change from linear to saturation smoothly.

For the drift region (region II);

$$\mathbf{Q_A}(\mathbf{V_x}) = -\mathbf{C_{ox}}(\mathbf{V_{G2}} - \mathbf{V_{x2}} - \boldsymbol{\emptyset_{ms2}}) \quad (15)$$

$$\mathbf{Q_{B2}}(\mathbf{V_x}) = -\mathbf{q}\,\mathbf{N_{drift}}(\mathbf{W_{d2,effective}}) = -\mathbf{q}\,\mathbf{N_{drift}}(\mathbf{d_2} - \mathbf{W_{d2}}(\mathbf{V_x})) \quad (16)$$

$$\mathbf{W_{d2}}(\mathbf{V_x}) = \sqrt{\frac{2\epsilon_s\,(\mathbf{V_D} - \mathbf{V_{x2}} - \mathbf{V_{bi}})}{\mathbf{q}\,\mathbf{N_{drift}}}} \quad (17)$$

The current in the region II (drift region) is due to two components; accumulated charges at the surface and bulk charges.

$$\mathbf{I_{D2}} = \frac{\mathbf{W}}{\mathbf{L_2}}\int_{\mathbf{V_{Di}}}^{\mathbf{V_D}} \boldsymbol{\mu}\,(-\mathbf{Q_A}(\mathbf{V_x}))\,\mathbf{dV_x} + \frac{\mathbf{W}}{\mathbf{L_2}}\int_{\mathbf{V_{Di}}}^{\mathbf{V_D}} \boldsymbol{\mu}\,(-\mathbf{Q_{B2}}(\mathbf{V_x}))\;\mathbf{dV_x} \quad (18)$$

Assuming the electron mobilities are the same for accumulated charges and bulk charges.

Substituting (15) to (17) in (18) and simplifying;

$$\mathbf{I_{D2}}(\mathbf{V_{Di}}) = \frac{\mathbf{W}}{\mathbf{2\,L_2}}\,\boldsymbol{\mu}\,\mathbf{C_{ox}}\left\{(\mathbf{2\,V_{G2}} - \boldsymbol{\emptyset_{ms2}})(\mathbf{V_D} - \mathbf{V_{Di}}) - \left(\mathbf{V_D^2} - \mathbf{V_{Di}^2}\right)\right\} + \frac{\mathbf{W}}{\mathbf{L_2}}\,\mathbf{q}\,\mathbf{N_{drift}}\mathbf{d_2}(\mathbf{V_D} - \mathbf{V_{Di}}) - \mathbf{0.67}\,\frac{\mathbf{W}}{\mathbf{L_2}}\boldsymbol{\gamma_2}\,\boldsymbol{\mu}\,\mathbf{C_{ox}}\{(\mathbf{V_D} - \mathbf{V_{Di}} - \mathbf{V_{bi}})^{1.5} + \mathbf{V_{bi}^{1.5}}\} \quad (19)$$

Equating equations (14) and (19) and solving for $\mathbf{V_{Di}}$. Then the current can be obtained by substituting $\mathbf{V_{Di}}$ in either equation (14) or (19).

3. Results

2D simulations for current-voltage characteristics and capacitances have been performed using Sentaurus from Synopsys [13]. Drift-diffusion model is employed in 2D simulations. Fig. 2 & 3 shows drain current versus Gate 1 voltage for different Gate 2 voltage values and for both VD = 0.1, 5 V. It is clear that when increasing the bias of Gate 2, the drain current increases. This is an indication of decreasing effective drift resistance value because of accumulating more charges at the surface of region II (drift region).

Also different capacitances versus Gate 1 voltage has been plotted for different Gate 2 biases and drain voltage biases. It is shown in Fig. 4 that Gate Capacitance $\mathbf{C_{GG}}$ in fF is plotted versus Gate 1 voltage in Volts for different Gate 2 voltage values $\mathbf{V_{G2}} = \mathbf{2, 4, and\ 6\ V}$ and $\mathbf{V_D} = \mathbf{0.1\ V}$. It is clear that increasing Gate 2 bias causes Gate Capacitance $\mathbf{C_{GG}}$ to increase with a considerable amount. This is because more carriers are available in the drift region when increasing Gate 2 voltage and that contributes to increasing capacitance. One comment to note here that for each curve there is a high change in capacitance value due to increasing Gate 1 voltage passing through threshold point as a lot of charges will start to flow so as increasing capacitance value.

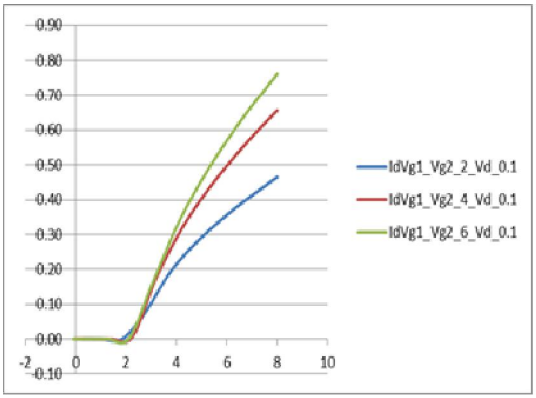

Figure 2. Drain current in mA versus Gate 1 voltage in Volts for different Gate 2 voltage values $V_{G2} = 2, 4,$ and 6 V **and** $V_D = 0.1$ V

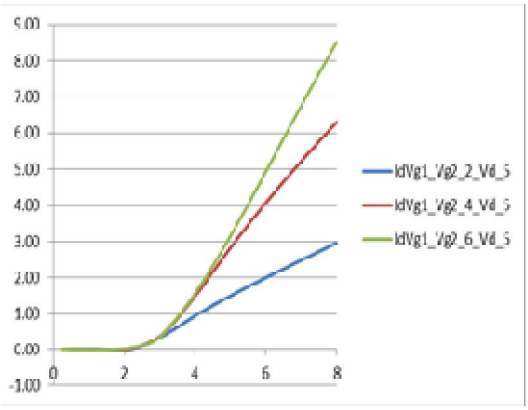

Figure 3 Drain current versus Gate 1 voltage for different Gate 2 voltage values $\mathbf{V_{G2} = 2, 4,}$ **and 6 V and** $\mathbf{V_D = 5}$ **V**

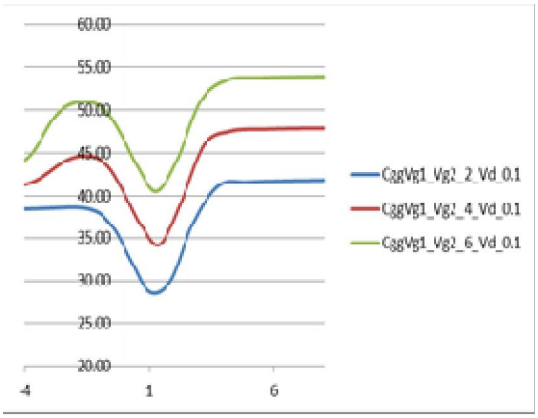

Figure 4 Gate Capacitance C_{GG} in fF versus Gate 1 voltage in Volts for different Gate 2 voltage values $V_{G2} = 2, 4,$ and 6 V **and** $V_D = 0.1$ V

However, when looking at Gate Capacitance C_{GG} behavior for higher drain voltage of 5 V per figure 5, the amount of change in capacitance is less at the region close to threshold because amount of change in charge is not so high while increasing Gate 2 voltage.

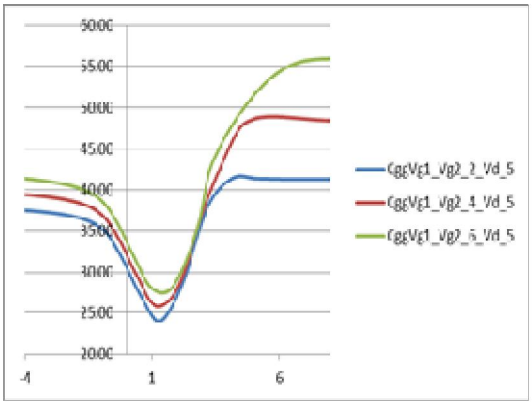

Figure 5 Gate Capacitance C_{GG} in fF versus Gate 1 voltage in Volts for different Gate 2 voltage values $V_{G2} = 2, 4,$ and 6 V **and** $V_D = 5$ V

For figure 6, it is shown that the peaks will be followed by saturation in the value of gate to drain capacitance and this peaks become less sharp when increasing Gate 2 voltage. This can be explained as when increasing Gate 2 voltage, drift region becomes less resistive so approaching the MOSFET case where no sharp peaks exists.

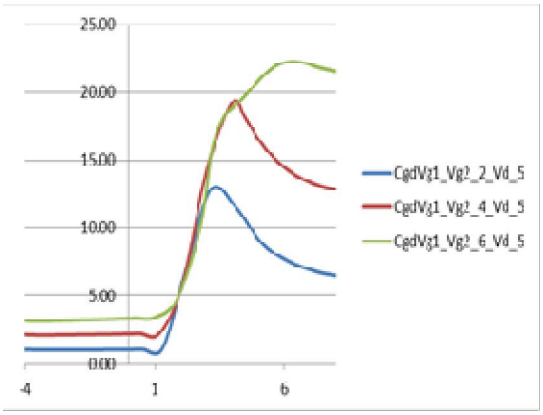

Figure 6 Gate to Drain Capacitance $\mathbf{C_{GD}}$ in fF versus Gate 1 voltage in Volts for different Gate 2 voltage values $\mathbf{V_{G2} = 2, 4,}$ **and 6 V and** $\mathbf{V_D = 5}$ **V**

Figure 7 shows for gate to drain capacitance that when operating way above threshold, the peak is reduced when increasing drain voltage. This is because the difference between Gate 2 voltage and drain voltage is higher so affecting depletion at drain.

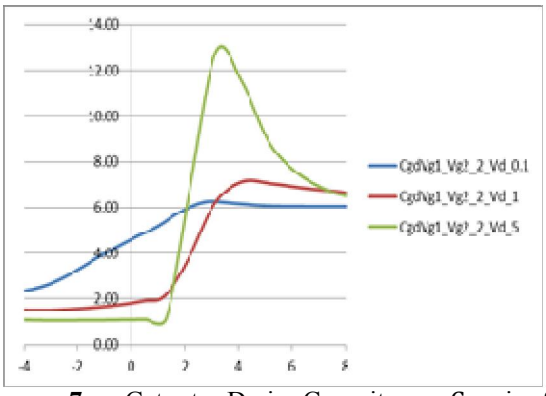

Figure 7 Gate to Drain Capacitance C_{GD} in fF versus Gate 1 voltage in Volts for different Gate 2 voltage values $V_D = 0.1, 1, \text{and } 5\ V$ and $V_{G2} = 2\ V$

4. Conclusion

A model has been developed for double-gate LDMOSFET high-voltage transistor, where the effect of a separately biased second gate is investigated. Current and capacitances have been studied with respect to bias of second gate. The results showed that increasing bias of the second added gate increases the current as an indication of reducing effective drift resistance. The gate capacitance increases considerably around threshold with increasing bias of Gate 2 for a low drain bias while its increase is smaller for a high drain bias. As for the gate to drain capacitance it increases with Gate 2 bias and its peak happens at higher Gate 2 bias. The increases for all capacitances are due primarily to the accumulation of more charges at the drift region.

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