A Systematic Synthesis for High-OrderSquare-Root Domain Filters with Reduced Voltage

Gwo-Jeng Yu
Department of Computer Science and information Engineering, Cheng Shiu University Niaosong, Taiwan 833, R. O. China. gjyu@csu.edu.tw

Received February 2, 2008

Abstract

A systematic synthesis for high-order square-root domain filter (SRD) based on the quadratic *I-V* relationship for an MOSFET operated in saturation region is presented in this paper. Emphases are placed on the methodology of filter synthesis, the constructive settings of DC components for input signals, the DC voltages of the state-space variables, and the DC bias current I_0. The proposed prototypes of square-root domain filters are able to overcome the possible inequality between the input and output node of DC level, in which improve the reliability of high-order filter implementation. Furthermore, by means of adjusting the range of the DC bias current I_0 in the acceptable boundary, the center frequency f_0 or 3 dB frequency f_{3dB} of the proposed prototypical circuits of SRD filters are not only attainable at megahertz frequencies but also tunable electronically. Simulations are performed with the model of a 0.25 μm CMOS process at 1.5 V supply voltage. The simulated results, which provide that the average errors of frequency response are smaller than 1.0%, demonstrate the validity of the proposed synthetic technique. The synthesized filters have the features of high frequency operation, tuneability, extensibility, and low power consumption. [Life Science Journal. 2010; 7(1): 15-29] (ISSN: 1097 – 8135)

Key Words: high-order square-root domain filter; low-voltage level-shift current mirror; current-mode square-root circuit; electronically tunable; high frequency operation; extensibility

Introduction

Today, many researchers have dedicated to developing companding filters which comprise log-domain and square-root domain (SRD) filters. Log-domain filter which was originally proposed by Adams[1] is a nonlinear (exponential) mapping on the state variables of a state-space (SS) description of a linear transfer function and includes the characteristics of high-frequency operation and tuneability. Frey[2-3] further utilized the exponential transformation of the state-space description of a linear transfer function, in terms of bipolar circuits, to implement log-domain filters and in turn, was embedded in as forming part of a broader branch of structures by Tsividis[4]. Furthermore, Drakakis et al.[5-7] proposed a systematic synthesis method, based on "Bernoulli cell", to realize the log-domain filters.

Most of the IC fabrication technologies, however, trend to digital CMOS processes, and this is due to the fact that a similar I–V exponential relationship holds the concept of "log-domain filtering" has been extended to the MOS transistors in weak-inversion region. Thus, adopting a direct transformation of the corresponding implementations based on bipolar transistors into MOS transistors realizations. To meet such demand and change, Toumazou et al.[8]and Germanovix et al.[9] proposed log-domain filters in terms of MOSFET circuits that operate in weak inversion. The main drawbacks of these topologies are the increased effect of transistor mismatches and the limited operation frequency, both originated from the operation mode of MOS transistor. As a result, the problems of the above methods are solved and enhanced via adopting the quadratic I–V relationship for the MOS transistor that operates in saturation region to implement log-domain filters-reducing fabrication cost while also lessening drawbacks such as high power supply voltage, high power consumption and low operation frequency. The methods are according to those of Eskiyerli et al.[10, 14], Yu et al.[11-12] and Lopez-Martin[13]. For this reason, these filters are also known as square-root domain filters. The basic building blocks for these filters include current mirrors, current-mode geometric-mean and multiplier-divider circuits. Different topologies for the geometric-mean circuits based on stacked MOS translinear loop[14-17]and up-down MOS translinear loop [18-19] are available in the open literature. Furthermore, both geometric mean and squarer blocks are used to implement the current-mode multiplier-divider[18-19].

For reliable operation of submicron digital CMOS integrated circuits, the continuous supply voltage decrease has become notable. Some current mirrors (CMs) are currently in use in most applications[20-22], whereas most of CMs either reveal severe performance degradation or are not functional at all in a low voltage supply environment. All high impedance CMs proposed by Mulder et al.[23], Zeki et al.[24] and Blalock et al.[25] require high input voltage, which provide the capability of high output voltage signal swing. The CMs proposed by[26-28] operate with low input voltage, whereas the main disadvantage of Prodanov et al.[26] has limited current range, Heim et al.[27] is not suitable for high frequency applications, and partial transistors of Itakura et al.[28] are biased in triode mode such that the mirror is sensitive to

geometry and threshold voltage mismatches.

Hence, Lopez-Martin et al.[29-30] proposed 1.5 V CMOS square-root domain low-pass and companding filters. The operation frequencies, nonetheless, remain low. In Yu et al.[31-32], an experiment based on 1.5 V square-root domain band-pass filter is proposed based on the MOSFET square law which contains the following characteristics and advantages: low cost, high frequency operation, low supply voltage operation, low power consumption, low noise, and electronically tunable of center frequency.

In this paper, based on the proposed prototypical circuits of SRD filters, a systematic synthesis method of high-order SRD filters is presented. Furthermore, in order to verify the extensibility of high-order filters, the synthetic procedures are also presented and discussed in which principles must be paid attention to at time of the syntheses for high-order filters, for example, the aspect ratios W/L of transistors, capacitance C, quality factor Q, DC bias voltages of driving MOSs, and DC bias current, etc. The main objectives are not only the demonstration of practicability of high-order low-voltage SRD filters, but also indicate the design matter requiring attention of the high-order filters.

Simultaneously, the simulated results of syntheses for several high-order low-voltage SRD filters are performed and compared with the specified values in which demonstrate the validity of the proposed synthetic technique and the high performances of the proposed prototypes of SRD filters.

Design Methodologies of Prototypes for Square-Root Domain filters

Square-root domain (SRD) filters feature a nonlinear (exponential) mapping on the state variables of a state-space description for a particular transfer function. In order to implement the filters, state equations must be further transformed to nodal equations at the nodes of grounded capacitors. Furthermore, based on the MOSFET square law relationship, the nodal equations are replaced by intermediate variables. Then, by means of interconnection of sub-circuits to realize the terms of nodal equation, the design procedures of square-root domain filters are achieved.

First, the transfer function of a band-pass filter (BPF) is introduced and shows how it is used to yield a SRD BPF. Assume that the transfer function of a second-order SRD BPF is expressed as

$$H(s)=\frac{\left(\frac{\omega_0}{Q}\right)s}{s^2+\left(\frac{\omega_0}{Q}\right)s+\omega_0^2} \tag{1}$$

and by using the standard technique[33-35] for creating companion-form dynamical equations, Eq. (1) is realized by the system described by the following equations.

$$\begin{cases} \dot{x}_1=-\omega_0 x_2 \\ \dot{x}_2=\omega_0 x_1-\left(\frac{\omega_0}{Q}\right)x_2+\left(\frac{\omega_0}{Q}\right)u \\ y=x_2 \end{cases} \tag{2}$$

where x_1, x_2, y, and u are state variables, output and input signals, respectively. Let the node voltages V_1 and V_2 be the state variables x_1 and x_2, and a voltage signal U denotes the input u, then (2) is rewritten as follows

$$\begin{cases} C\dot{V}_1=-C\omega_0 V_2 \\ C\dot{V}_2=C\omega_0 V_1-(\frac{C\omega_0}{Q})V_2+(\frac{C\omega_0}{Q})U \\ y=V_2 \end{cases} \tag{3}$$

with C is a multiplying factor. Both of $C\dot{V}_1$ and $C\dot{V}_2$ in (3) are regarded as the time-dependent current through the two capacitors C connected between V_1 and ground and between V_2 and ground, respectively.

Assume that the drain current of an MOSFET transistor operated in saturation region is expressed as

$$I_D=\frac{\mu_0 C_{ox} W}{2L}(V_{GS}-V_T)^2=\beta(V_{GS}-V_T)^2 \tag{4}$$

where β, V_{GS}, and V_T are the device transconductance parameter, the gate-to-source voltage, and the threshold voltage, respectively.

Hence, based on (4), the state equations of Eq.(3) are transformed into [11-12, 31-32]

$$\begin{cases} C\dot{V}_1=-\sqrt{I_0 I_2}-I_T \\ C\dot{V}_2=\sqrt{I_0 I_1}-\frac{\sqrt{I_0 I_2}}{Q}+\frac{\sqrt{I_0 I_U}}{Q}+I_T \\ y=V_2 \end{cases} \tag{5}$$

where

$$I_1\equiv\beta(V_1-V_T)^2 \tag{6}$$

$$I_2\equiv\beta(V_2-V_T)^2 \tag{7}$$

$$I_U\equiv\beta(U-V_T)^2 \tag{8}$$

$$I_T \equiv C\omega_0 V_T \tag{9}$$

and

$$I_0 \equiv \frac{C^2\omega_0^2}{\beta} \quad \text{or} \quad f_0 = \frac{\omega_0}{2\pi} = \frac{\sqrt{\beta I_0}}{2\pi C} \tag{10}$$

Note that (6)-(10) are defined as the currents in the circuit corresponding to input voltages V_1, V_2, U, the DC compensation term of the threshold voltage V_T and the DC bias current, respectively. The SRD BPF is driven by the external applied input voltage U and DC bias current I_0. Hence, based on the given device parameters β and V_T of the transistors, the capacitance C, the DC bias current I_0, and the quality factor Q, the center frequency f_0 and the DC compensation current I_T can be calculated. Moreover, the current I_U is also yielded to correspond to the input voltage U. However, the currents I_1 and I_2 are changed according to the variations of the node voltages V_1 and V_2. The output is then taken from the node voltage V_2.

The center frequency f_0, defined in (10), is proportional to the square root of the DC bias current I_0, whereas is inversely proportional to the capacitance C. Therefore, the center frequency f_0 is tuned by using the capacitance C and the DC bias current I_0.

Similar to the above methodologies, the equivalent representations for first-order and second-order SRD filters may be derived as listed in Table 1.

Next, in order to achieve low voltage circuit operation, both of the n-type and n-type low-voltage (LV) current mirrors (CMs) in the proposed SRD filters are designed by means of LV level-shift technique, as shown in Fig. 1[32]. Simultaneously, Fig. 2[32] shows the DC biasing circuit diagrams of the proposed n-type and p-type LV level-shift CMs, respectively, where V_{N1}, V_{N2}, V_{P1}, and V_{P2} are connected to the corresponding bias terminals of the CMs, such that the overall supply voltage source is simplified to be only one supply voltage source V_{DD}.

Table 1. Equivalent representations of the SRD filters.

Types of filters	Transfer functions	State equations	Equivalent equations of KCL
Second-order band-pass filter	$H(s) = \frac{\left(\frac{\omega_0}{Q}\right)s}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}$	$\begin{cases} \dot{x}_1 = -\omega_0 x_2 \\ \dot{x}_2 = \omega_0 x_1 - \left(\frac{\omega_0}{Q}\right)x_2 + \left(\frac{\omega_0}{Q}\right) \\ y = x_2 \end{cases}$	$\begin{cases} C\dot{V}_1 = -\sqrt{I_0 I_2} - I_T \\ C\dot{V}_2 = \sqrt{I_0 I_1} - \frac{\sqrt{I_0 I_2}}{Q} + \frac{\sqrt{I_0 I_U}}{Q} + I_1 \\ y = V_2 \end{cases}$
First-order low-pass filter	$H(s) = \frac{\omega_0}{s + \omega_0}$	$\begin{cases} \dot{x} = -\omega_0 x + \omega_0 u \\ y = x \end{cases}$	$\begin{cases} C\dot{V}_1 = -\sqrt{I_0 I_1} + \sqrt{I_0 I_U} \\ y = V_1 \end{cases}$
Second-order low-pass filter	$H(s) = \frac{\omega_0^2}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}$	$\begin{cases} \dot{x}_1 = -\omega_0 x_2 + \omega_0 u \\ \dot{x}_2 = \omega_0 x_1 - \left(\frac{\omega_0}{Q}\right)x_2 \\ y = x_2 \end{cases}$	$\begin{cases} C\dot{V}_1 = -\sqrt{I_0 I_2} + \sqrt{I_0 I_U} \\ C\dot{V}_2 = \sqrt{I_0 I_1} - \left(\frac{\sqrt{I_0 I_2}}{Q}\right) + \left(1 - \frac{1}{Q}\right)I \\ y = V_2 \end{cases}$
Second-order biquad filter	$H_1(s) = \frac{y}{u_1} = \frac{\omega_0^2}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}$ $H_2(s) = \frac{y}{u_2} = \frac{\left(\frac{\omega_0}{Q}\right)s}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}$	$\begin{cases} \dot{x}_1 = -\omega_0 x_2 + \omega_0 u_1 \\ \dot{x}_2 = \omega_0 x_1 - \left(\frac{\omega_0}{Q}\right)x_2 + \left(\frac{\omega_0}{Q}\right) \\ y = x_2 \end{cases}$	$\begin{cases} C\dot{V}_1 = -\sqrt{I_0 I_2} + \sqrt{I_0 I_{U1}} \\ C\dot{V}_2 = \sqrt{I_0 I_1} - \frac{\sqrt{I_0 I_2}}{Q} + \frac{\sqrt{I_0 I_{U2}}}{Q} + I \\ y = V_2 \end{cases}$

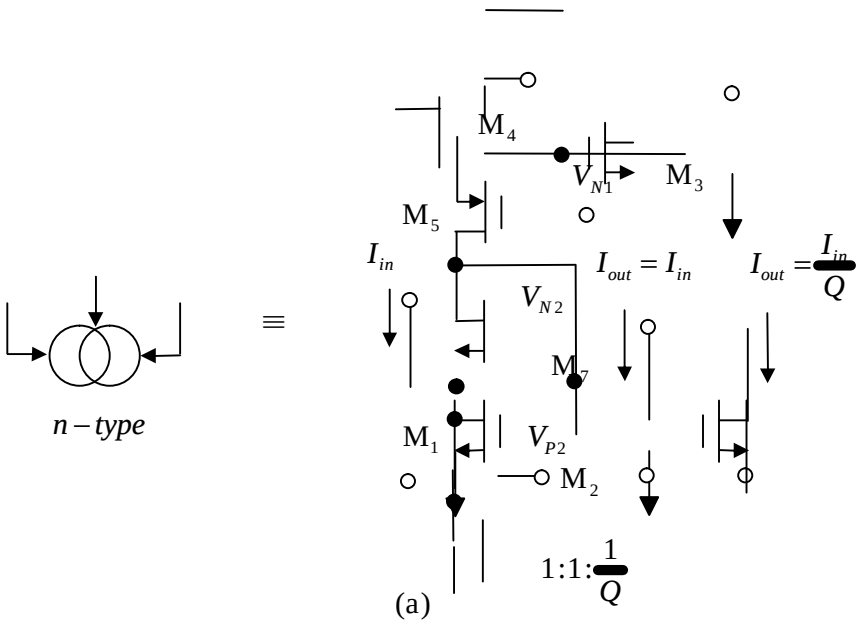


Fig. 1. (a) Symbol and circuit diagram of the n-type LV level-shift CM, (b) Symbol and circuit diagram of the p-type LV level-shift CM.

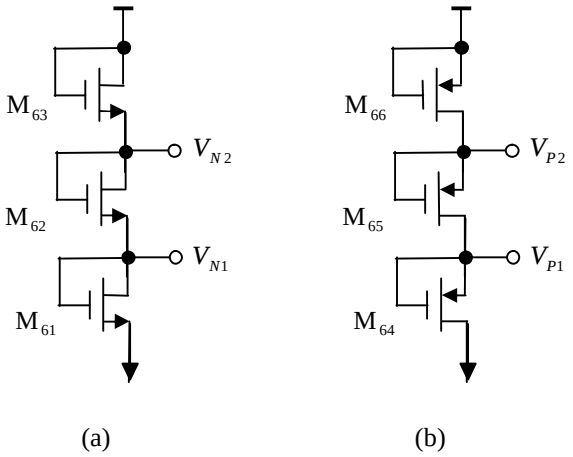


Fig. 2. DC biasing circuit diagram of (a) n-type and (b) p-type LV level-shift CMs.

Note that, in Fig. 1(a), the transistor M_5 biased by a voltage V_{N1} is acted as a current source. The V_{DS} voltage of transistor M_1 is fixed to a constant value by transistor M_4, current source transistor M_5, and voltage source V_{N2}. The transistor M_4 with bias voltage V_{N2} provides shunt feedback to form lower input impedance, which reduces the input voltage requirement.

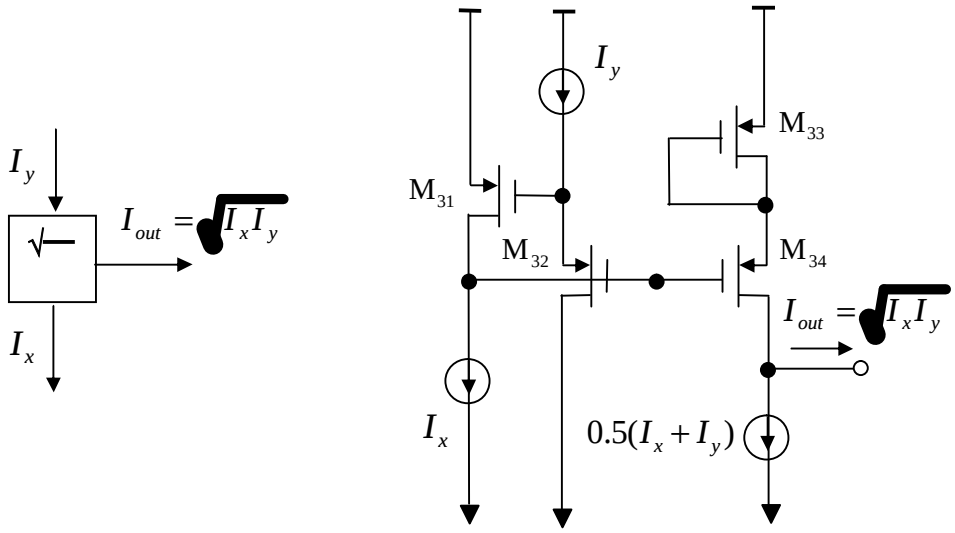
Further, according to the MOSFET square law, the square-root of two currents is realized by the current-mode square-root circuit as shown in Fig. 3[32]. The core circuit is composed of transistors M_{31}, M_{32}, M_{33}, and M_{34}. The other transistors except M_{31}-M_{34}, which are the LV level-shift CMs, are used to transmit current signals. Assume that the aspect ratios of the transistors in core circuit satisfy the following constraints:

$$\beta_{31} = \beta_{32} \equiv \beta \text{ and } \beta_{33} = \beta_{34} \equiv 2\beta \quad (11)$$

Thus, from the derivations of[31-32], we have

$$I_{out} = \sqrt{I_x I_y} \quad (12)$$

which conforms to the function of the current-mode square-root circuit.



(a) (b)

Fig. 3. (a) Symbol of the current-mode square-root circuit, (b) circuit diagram of the current-mode square-root circuit.

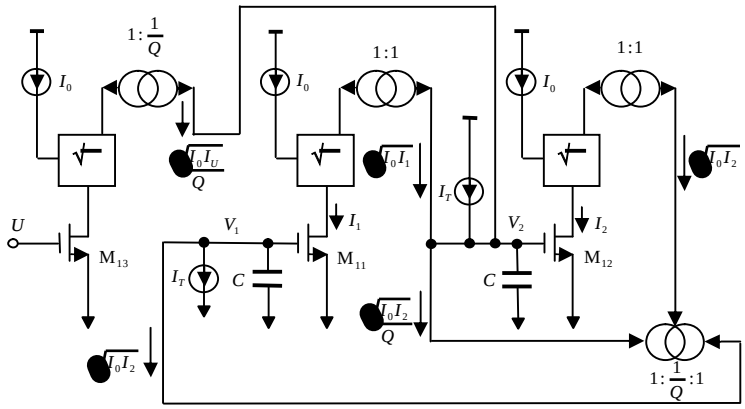


Fig. 4. Prototypical circuit of the proposed second-order LV SRD BPF.

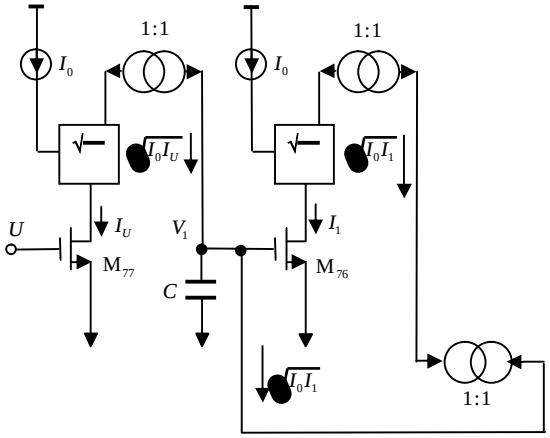


Fig. 5. Prototypical circuit of the proposed first-order LV SRD LPF.

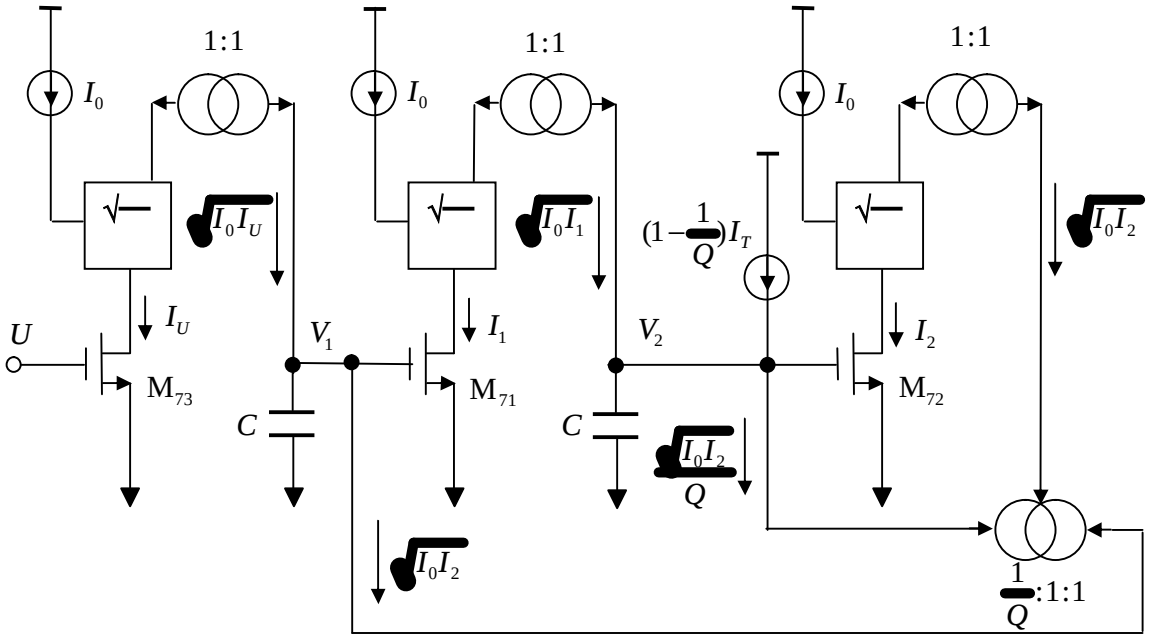


Fig. 6. Prototypical circuit of the proposed second-order LV SRD LPF.

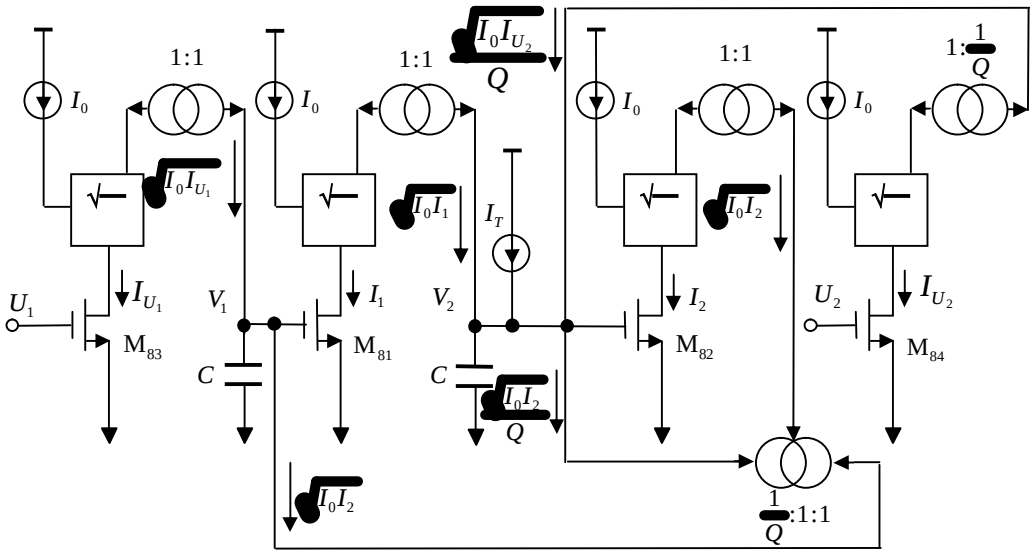


Fig. 7. Prototypical circuit of the proposed second-order LV SRD biquad.

Obviously, the constraint for the minimum power supply voltage V_{DD} is determined by following conditions,

$$V_{DD} \geq 2V_{EFP} + V_{EFN} \quad (13)$$

$$V_{DD} \geq 2V_{EFP} + |V_{TP}| \quad (14)$$

$$V_{N1} = \frac{V_{DD} + \left(\sqrt{(\frac{W}{L})_{61}/(\frac{W}{L})_{62}} + \sqrt{(\frac{W}{L})_{61}/(\frac{W}{L})_{63}} - 2\right)V_{TN}}{\left(\sqrt{(\frac{W}{L})_{61}/(\frac{W}{L})_{62}} + \sqrt{(\frac{W}{L})_{61}/(\frac{W}{L})_{63}} + 1\right)} \quad (15)$$

$$V_{N2} = V_{N1} + V_{TN} + \left(\sqrt{(\frac{W}{L})_{61}/(\frac{W}{L})_{62}}\right)(V_{N1} - V_{TN}) \quad (16)$$

where V_{TN} and V_{TP} are the threshold voltage of the NMOS and PMOS transistor, respectively, $V_{EFN} \equiv V_{GSN} - V_{TN}$ and $V_{EFP} \equiv V_{SGP} - |V_{TP}|$ are defined as the minimum source-to-drain voltages required to sustain an NMOS transistor and PMOS transistor in saturation, respectively.

Hence, the prototypical circuit of the proposed second-order LV SRD BPF expressed as (5) is realized by using the LV level-shift CMs, three current-mode square-root circuit blocks, and two capacitors, as shown in Fig. 4[32], where U and I_0 are the external applied DC biasing input voltage and DC biasing current, respectively, and V_2 is the desired output voltage. Furthermore the currents I_U, I_1, and I_2 in the BPF are related to the corresponding input voltages U, V_1, and V_2, respectively. The DC bias current I_0 is used to control the position of center frequency of this BPF. As evident, the BPF having the expected transfer function may operate at lower supply voltage.

Similar to the above technologies, the prototypical circuits for proposed first-order LV SRD LPF, second-order LV SRD LPF, and second-order LV SRD biquad may be given, which are shown in Figs. 5, 6, and 7[32], respectively. Simultaneously, Figs. 1 to 7 are regarded as prototypes (or basic block diagrams) while carrying out the syntheses of high-order LV SRD filters.

Furthermore, consider the proposed circuits based on TSMC 0.25 μm 1p5m CMOS process with $V_{TN} = 0.53\,\text{V}$ and $|V_{TP}| = 0.58\,\text{V}$ to verify the functions of the proposed second-order LV SRD BPF. The maximum operation current is 200 μA, the power supply voltage V_{DD} for the proposed LV SRD BPF as shown in Fig. 4 is set as 1.5 V, and two capacitors in this BPF are $C_1 = C_2 = 0.9$ pF. The DC biasing voltages of V_{N1}, V_{N2}, V_{P1}, and V_{P2} under $V_{DD} = 1.5$ V are measured to be 0.52 V, 1.02 V, 0.95 V and 0.46 V, respectively. The microphotograph of the proposed second-order LV SRD BPF is shown in Fig. 8 where the total area of this filter is 0.0175 mm^2.

Table 2 shows the measured and simulated results for the proposed LV SRD BPF and LPF, respectively; Table 3 shows the simulated results for the proposed LV SRD biquad filter[32]. Both of the measured and simulated results for the proposed LV SRD BPF are in well agreement and demonstrate that the center frequency f_0 are tunable electronically, further indicate that the proposed circuit is able to provide reliable operation at 1.5 V with low power consumption and high noise immunity.

Systematic Synthesis for High-Order Square-Root Domain Filters

Assume that the circuit diagrams of LV current-mode level-shift CMs, square-root circuit, the first-order and second-order LV SRD filters shown in Figs. 1 to 7 are regarded as the prototypes (or basic block diagrams), then the transfer function of a high-order LV SRD filter can be decomposed into the product of several first-order and second-order ones, which can be implemented by cascading the corresponding prototypes.

Note that every individual pole frequency of the first-order or the second-order LV SRD filter must be adjusted to meet the specified pole frequency. Simultaneously, for realizing the high-order filter, the possible inequality between the input, output node, and grounded capacitors of DC level which will induce the incomplete power propagation and seriously degrade the frequency response of the filter all must be improved. Hence, in the course of designing, additional condition will be joined by setting the DC components of input signals and state-space variables to be a same DC voltage value, in order to guarantee that the DC levels of the input node, the output node, and the grounded capacitors are equal. Fig. 9 shows the synthetic procedures of high-order LV SRD filters in which the aspect ratios W/L of transistors for the current-mode CMs and square-root circuit shown in Table 4 are assumed to be fixed, while those of transistors and C for the current-mode LV SRD filters shown in Table 5 are allowed to be adjustable such that the DC bias current I_0 may fall into the acceptable boundary which are demonstrated in the simulated and measured results of[32].

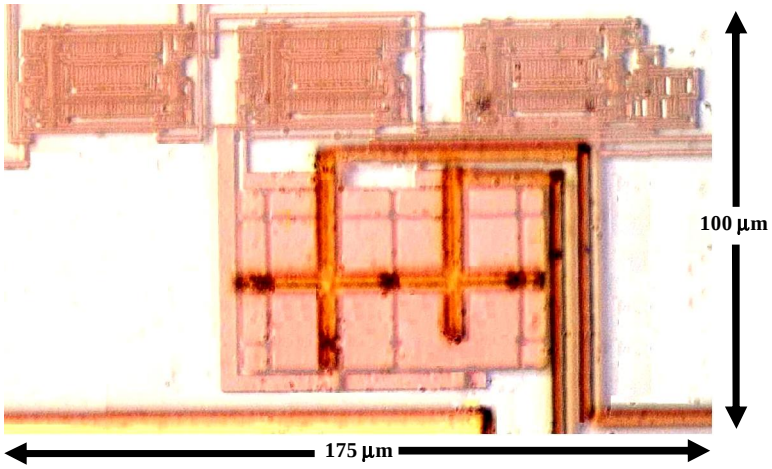


Fig. 8. The microphotograph of the proposed second-order LV SRD BPF.

Table 2. Measured and simulated results for the proposed LV SRD BPF and LPF.

Parameters	LV SRD BPF Measured results	LV SRD LPF Simulated results	LV SRD LPF Simulated results
Technology	TSMC 0.25 µm 1p5m		
Order of the filter	2	1	2
Q	21.3	1	1
C	0.9 pF	1 pF	1 pF
Supply voltage	1.5 V	1.5 V	1.5 V
Power consumption (average)	1.598 mW	0.366 mW	0.633 mW
f_0 or f_{3dB} tuning range	f_0 = 4 - 10 MHz	f_{3dB} = 1.2 – 21.2 MHz	f_{3dB} = 1.1 – 22.5 MHz
IM3 (V_{pp} = 0.1 V)	-44.67 dB (5.35 MHz and 5.4 MHz (in band))	-45.3 dB (4 MHz and 5 MHz (in band))	-38.6 dB (4 MHz and 5 MHz (in band))
THD (V_{pp} = 0.1 V)	-26.7 dB (5.38 MHz)	-27.6 dB (1 MHz)	-26.0 dB (1 MHz)
Output noise power	-45.2 dBm	-46.2 dBm	-44.2 dBm
SFDR	35.0 dB	37.1 dB	34.6 dB
Measured and simulated conditions			
I_0	90 µA	20 µA	20 µA
f_{3dB}	5.52 MHz	13.7 MHz	14.4 MHz
f_0	5.66 MHz		

Table 3. Simulated results for the proposed second-order LV SRD biquad filter.

Parameters	Simulated results	
	Band-pass section	Low-pass section
Technology	TSMC 0.25 µm 1p5m	TSMC 0.25 µm 1p5m
Order of the filter	2	2
Q	1	1
Supply voltage	1.5 V	1.5 V
Power consumption (average)	1.42 mW	1.27 mW
f_0 or f_{3dB} tuning range	f_0 = 1.9 – 17.0 MHz	f_{3dB} = 1.2 – 22.2 MHz
IM3 (V_{pp} = 0.1 V)	-33.2 dB (10 MHz and 11 MHz (in band))	-34.1 dB (5 MHz and 6 MHz (in band))
THD (10 MHz,V_{pp} = 0.1V)	-25.2 dB	-24.8 dB
Output noise power	-43.7 dBm	-44.0 dBm
SFDR	32.7 dB	31.6 dB
Simulated conditions		
I_0	20 µA	20 µA
f_{3dB1}, f_0, f_{3dB2}	6.7 MHz, 10.2 MHz, 13.5 MHz	f_{3dB} = 14.1 MHz

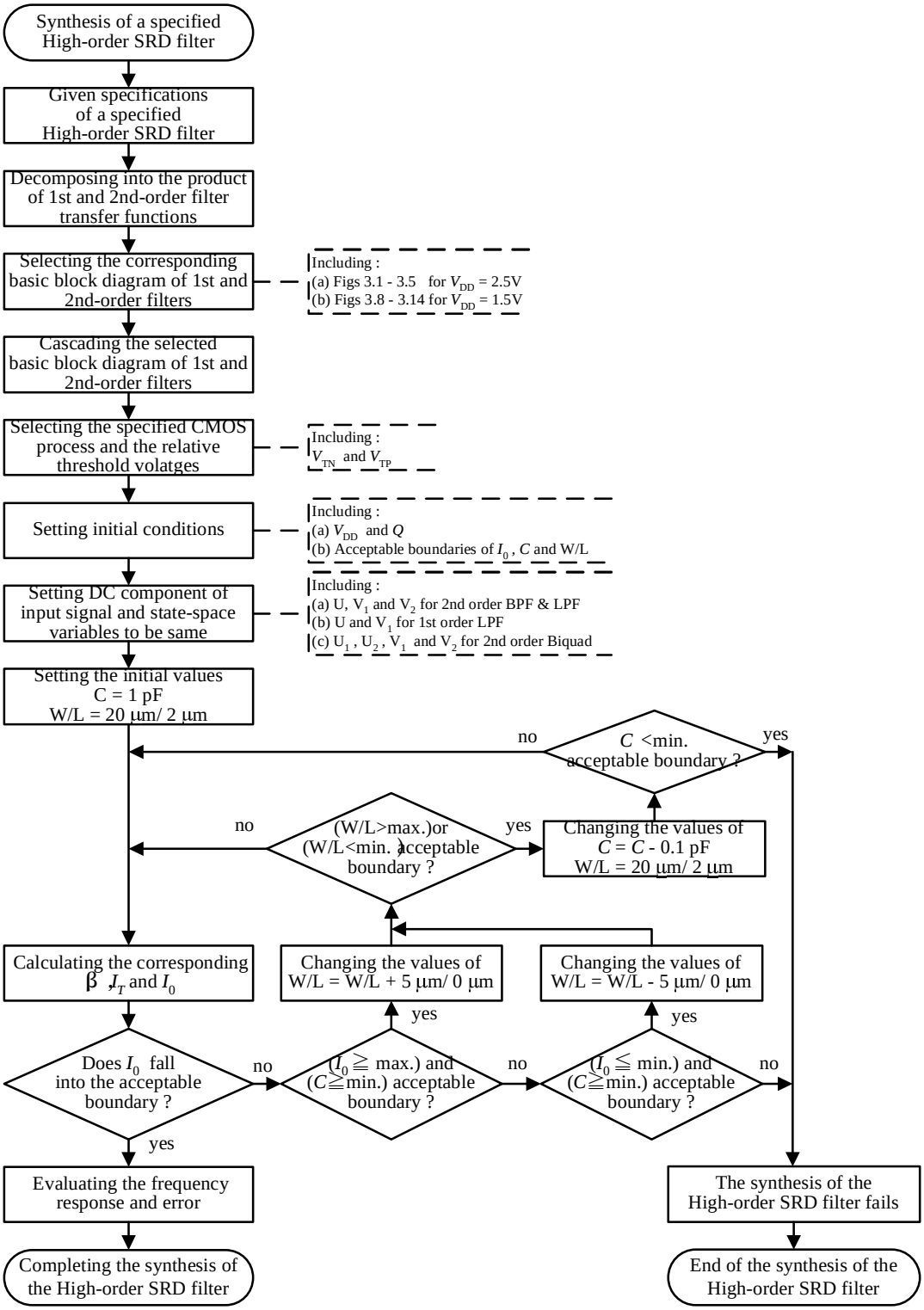


Fig. 9. The synthetic procedures of a specified high-order LV SRD filter.

Table 4. The aspect ratios of transistors for the LV current-mode level-shift CMs and square-root circuit shown in Figs. 1 to 3

Prototypes	The aspect ratios (W/L)
The proposed LV level-shift CMs (Fig. 1)	W/L = 20 m/2 m
The DC biasing circuits (Fig. 2)	$(W/L)_{61}$ = 2 m/0.25 m, $(W/L)_{62}$ = 0.3 m/0.25 m, $(W/L)_{63}$ = 0.3 m/0.25 m, $(W/L)_{64}$ = 2 m/0.25 m, $(W/L)_{65}$ = 4 m/0.25 m, $(W/L)_{66}$ = 30 m/0.25 m
The proposed LV current-mode square-root circuits (Fig. 3)	W/L = 7 m/0.7 m except W/L = 14 m/0.7 m for M_{33} and M_{34}

Table 5. The acceptable boundaries of C, W/L, and I_0 of the LV current-mode LV SRD filters shown in Figs. 4 to 7 operated at V_{DD} = 1.5 V.

Type of filters	Prototypes	C	W/L	I_0
Second-order LV SRD BPF	Fig. 4	0.5 – 1.0 pF	10 m/2 m - 40 m/2 m for M_{11} - M_{13}	60 - 200μA
First-order LV SRD LPF	Fig. 5	0.5 – 1.0 pF	10 m/2 m - 40 m/2 m for M_{76} - M_{77}	2 - 40μA
Second-order LV SRD LPF	Fig. 6	0.5 – 1.0 pF	10 m/2 m - 40 m/2 m for M_{71} - M_{73}	2 - 40μA
Second-order LV Low-pass section of SRD biquad	Fig. 7	0.5 – 1.0 pF	10 m/2 m - 40 m/2 m for M_{81} - M_{84}	2 - 40μA
Second-order LV Band-pass section of SRD biquad	Fig. 7	0.5 – 1.0 pF	10 m/2 m - 40 m/2 m for M_{81} - M_{84}	2 - 40μA

Simulated Results of High-Order Square-Root Domain Filters

Consider the proposed prototypical circuits based on TSMC 0.25 μm 1p5m CMOS process with $V_{TN} = 0.53V$ and $|V_{TP}| = 0.58V$ to verify the functions of the proposed high-order LV SRD filters.

Synthesis of Third-Order LV SRD Low-Pass Filter

For an attempt to synthesize a third-order low-voltage square-root domain low-pass filter specified in Table 6, the synthetic configurations have two types that contain one stage of second-order LV SRD LPF cascaded one stage of first-order LV SRD LPF or one stage of second-order LV low-pass section of SRD biquad cascaded one stage of first-order LV SRD LPF shown in Fig. 10(a) and (b), respectively, whereas, the synthetic methods for the two configurations are similar. Thus, accordingly, only one of the synthetic configurations, one stage of second-order LV SRD LPF cascaded one stage of first-order LV SRD LPF, is provided in the following.

Table 6. Specifications of a third-order LV SRD LPF.

Parameters	Specifications
Technology	TSMC 0.25μm 1p5m
Order of the filter	3
Type of filter	Low-pass filter
Q	1
Supply voltage	1.5 V
3 dB frequency f_{3dB}	1.5 MHz

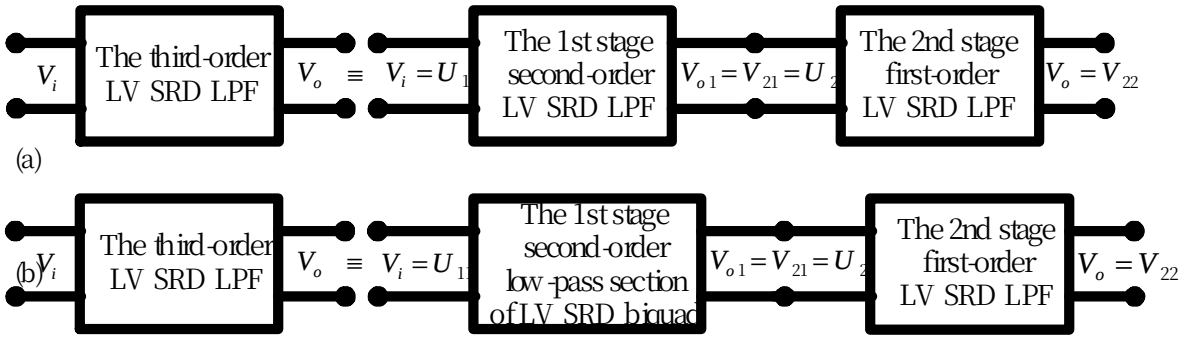


Fig. 10. Synthetic configurations of the specified third-order LV SRD low-pass filter.

Firstly, the prototypical circuits of second-order LV SRD LPF and first-order LV SRD LPF are given in Fig. 6 and 5, respectively, which the boundaries of I_0, C, and W/L are rewritten and given in Table 7. Thus, according to the synthetic procedures shown in Fig. 9, the initial values of C and W/L for the corresponding circuits are set to be C = 1 pF and W/L = 20 m/2 m, respectively, and let the DC components of input signal and state-space variables be $U = V_1 = V_2 = 0.65$ V. Next, the corresponding values of β, I_T, and I_0 defined in (4), (9), and (10), respectively, are identical for the two prototypical circuits as

$$\beta \equiv \frac{1}{2}\mu_0 C_{ox}\left(\frac{W}{L}\right) \approx 30.81\,\mu A/V^2$$

$$I_T \equiv C\omega_0 V_T = C\,(2\pi f_0)V_T \approx 5.00\,\mu A$$

$$I_0 \equiv \frac{C^2\omega_0^2}{\beta} = \frac{C^2\,(2\pi f_0)^2}{\beta} \approx 2.88\,\mu A$$

where the DC bias current I_0 falls into the acceptable boundary shown in Table 7. Hence, the simulated frequency response of third-order LV SRD LPF may be evaluated as shown in Fig. 11 in which the simulated 3 dB frequency f_{3dB} is approximately 1.486 MHz. Obviously the error of frequency response is approximately 0.933%, while compared with the specified 3 dB frequency f_{3dB} = 1.5MHz

Table 7. The acceptable boundaries of C, W/L, and I_0 of second-order LV SRD LPF and first-order LV SRD LPF.

Type of filters	Prototypes	C	W/L	I_0
Second-order LV SRD LPF	Fig. 6	0.5 – 1.0 pF	10μm/2μm - 40μm/2μm for M_{71} - M_{73}	2 - 40μA
First-order LV SRD LPF	Fig. 5	0.5 – 1.0 pF	10μm/2μm - 40μm/2μm for M_{76} - M_{77}	2 - 40μA

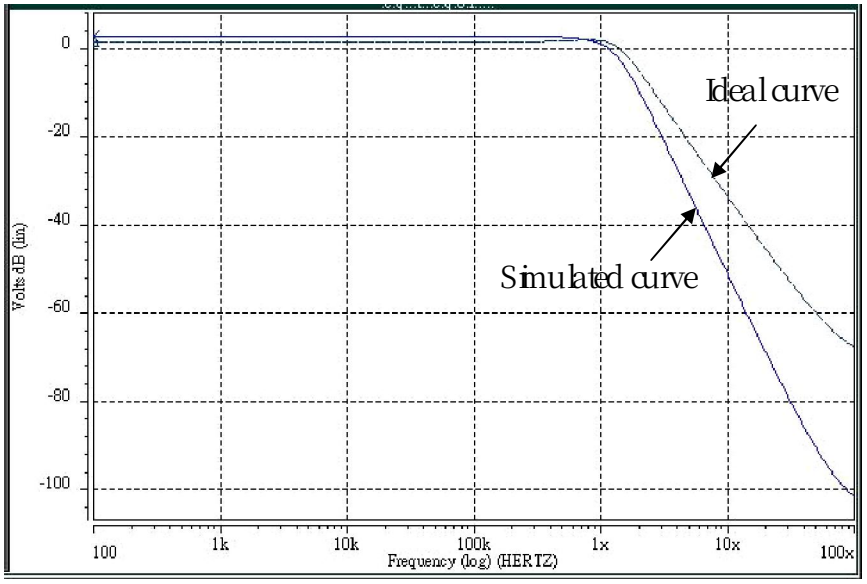


Fig. 11. The simulated frequency response of the third-order LV SRD LPF.

Synthesis of Eighth-Order LV SRD Band-Pass Filter

Similarly, by means of combining four stages second-order LV SRD BPF or LV band-pass section of SRD biquad cascaded, an eighth-order low-voltage square-root domain band-pass filter specified in Table 8 may be synthesized. Further, simply only the synthetic method of adopting four stages of second-order LV SRD BPF cascaded is described.

Table 8. Specifications of an eighth-order LV SRD BPF.

Parameters	Specifications
Technology	TSMC 0.25μm 1p5m
Order of the filter	8
Type of filter	Band-pass filter
Q	1
Supply voltage	1.5V
Center frequency f_0	5MHz

The adopted prototype of second-order LV SRD BPF shown in Fig. 4 and Table 9 is then the corresponding boundaries of I_0, C, and W/L. Furthermore, according to the synthetic procedures of Fig. 9, the initial values of C and W/L for the corresponding prototype are set to be 1 pF and 20 m/2 m, respectively, and assume the DC components to be $U = V_1 = V_2 = 0.65$ V. Hence, the corresponding values of β, I_T, and I_0 for the second-order LV SRD BPF are calculated as

$$\beta \approx 30.81 \ \text{V}^2,\ I_T \approx 16.65, \text{and } I_0 \approx 32.03$$

Table 9. The acceptable boundaries of C, W/L, and I_0 of second-order LV SRD BPF.

Type of filters	Prototypes	C	W/L	I_0
Second-order LV SRD BPF	Fig. 4	0.5 – 1.0 pF	10μm/2μm - 40μm/2μm for M_{11} - M_{13}	60 - 200μA

However, the DC bias current I_0 is smaller than the acceptable lower limit 60μA specified in Table 9. Thus, according to the synthetic procedures of Fig. 9, the aspect ratio W/L must be decreased to be W/L = 10μm/2 m. The resultant quantities are

$$\beta \approx 15.41\mu\text{A V}^2,\ I_T \approx 16.65, \text{and } I_0 \approx 64.05\mu\text{A}$$

which indicate DC bias current I_0 satisfies the acceptable boundary specified in Table 9. Hence, the simulated frequency response of the eighth-order LV SRD BPF is performed and shown in Fig. 12 in which the simulated center frequency f_0 approximates at 4.97 MHz and suffers from 0.6% error of frequency response, while compared with the specified center frequency f_0 = 5 MHz.

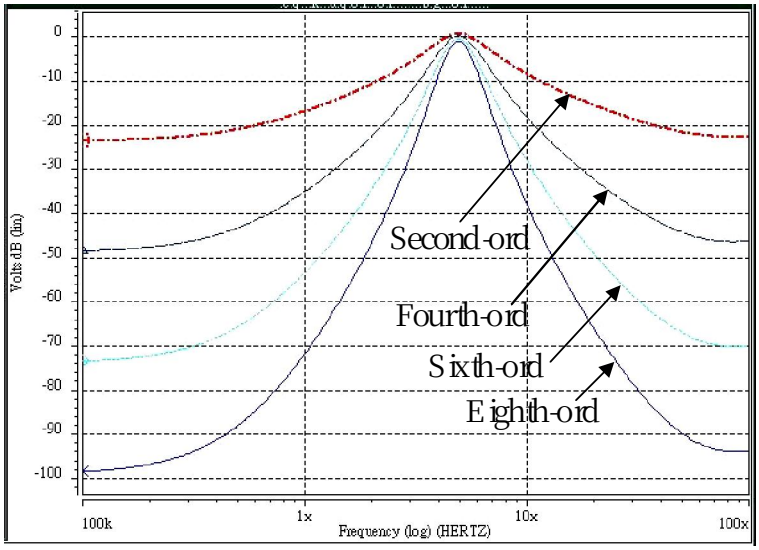


Fig. 12. The simulated frequency response of the eighth-order LV SRD BPF.

Synthesis of Ninth-Order LV SRD Low-Pass Filter

Next, in order to design a ninth-order LV SRD low-pass filter specified in Table 10, two schemes are used. Each contains four stages of second-order LV SRD LPF cascaded one stage of first-order LV SRD LPF or four stages of second-order LV low-pass section of SRD biquad cascaded one stage of first-order LV SRD LPF, respectively, are provided in below and demonstrated.

Table 10. Specifications of a ninth-order LV SRD LPF.

Parameters	Specifications
Technology	TSMC 0.25μm 1p5m
Order of the filter	9
Type of filter	Low-pass filter
Q	1
Supply voltage	1.5 V
3 dB frequency f_{3dB}	2 MHz

Four Stages of Second-Order LV LPF Cascaded One Stage of First-Order LV SRD LPF. The prototypes of second-order LV SRD LPF and first-order LV SRD LPF are given in Fig. 6 and 5, respectively, and the corresponding boundaries of I_0, C, and W/L are rewritten and given in Table 11. Simultaneously, the initial values of C and W/L for the corresponding prototypes are also set to be 1 pF and 20μm/2μm, respectively. Thus, the corresponding values of β, I_T, and I_0 for the two prototypes are all identical, result in

$\beta \approx 30.81\mu A/V^2$, $I_T \approx 6.66\mu A$, and $I_0 \approx 5.13\mu A$

where the DC bias current I_0 meets the acceptable boundary shown in Table 11. Fig. 13 shows the simulated frequency response of the ninth-order LV SRD LPF. The simulated 3 dB frequency f_{3dB} approximates at 2.018 MHz and results in approximately 0.9% error of frequency response.

Table 11. The acceptable boundaries of C, W/L, and I_0 of the second-order LV SRD LPF and first-order LV SRD LPF.

Type of filters	Prototypes	C	W/L	I_0
Second-order LV SRD LPF	Fig. 6	0.5 – 1.0 pF	10 μm/2μm - 40μm/2μm for M_{71} - M_{73}	2 - 40μA
First-order LV SRD LPF	Fig. 5	0.5 – 1.0 pF	10μm/2μm - 40μm/2μm for M_{76} - M_{77}	2 - 40μA

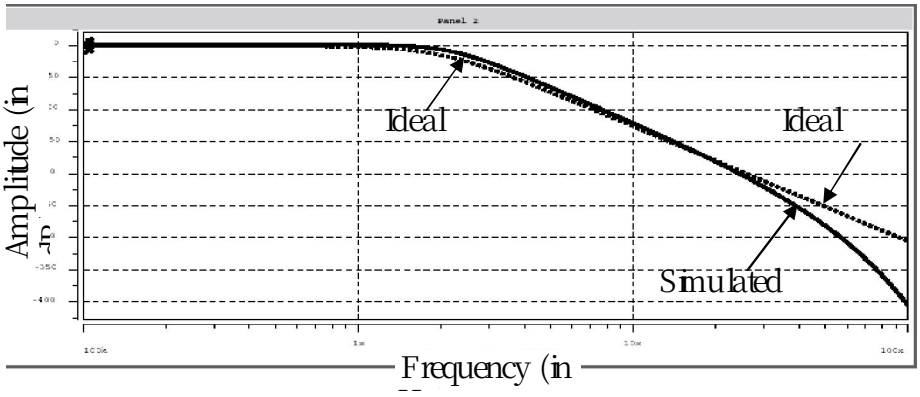


Fig. 13. The simulated frequency response of the ninth-order LV SRD LPF.

Four Stages of Second-Order LV Low-Pass Section of SRD Biquad Cascaded One Stage of First-Order LV SRD LPF

Similarly, Figs. 7 and 5 are adopted as the prototypes of second-order LV low-pass section of SRD biquad and first-order LV SRD LPF, respectively. Table 12 is the corresponding boundaries of I_0, C, and W/L. Next, the initial values of C and W/L for the corresponding prototypical circuits are set to be 1 pF and 20μm/2μm, respectively, and let the DC components be $U_1 = U_2 = V_1 = V_2 = 0.65$ V. Hence, the corresponding values of β, I_T, and I_0 for the two prototypical circuits are also identical and calculated as

$\beta \approx 30.81\mu A/V^2$, $I_T \approx 6.66\mu A$, and $I_0 \approx 5.13\mu A$

The DC bias current I_0 also falls into the acceptable boundary shown in Table 12. Hence, the simulated frequency response of the ninth-order LV SRD LPF is shown in Fig. 14. The simulated 3 dB frequency f_{3dB} approximates at 2.02 MHz and suffers from approximately 1.0% error of frequency response.

Table 12. The acceptable boundaries of C, W/L, and I_0 of the second-order LV low-pass section of SRD biquad and first-order LV SRD LPF.

Type of filters	Prototypes	C	W/L	I_0
Second-order LV low-pass section of SRD biquad	Fig. 7	0.5 – 1.0 pF	10μm/2μm - 40μm/2 m for M_{81} - M_{84}	2 - 40μA
First-order LV SRD LPF	Fig. 5	0.5 – 1.0 pF	10μm/2μm - 40μm/2μm for M_{76} - M_{77}	2 - 40μA

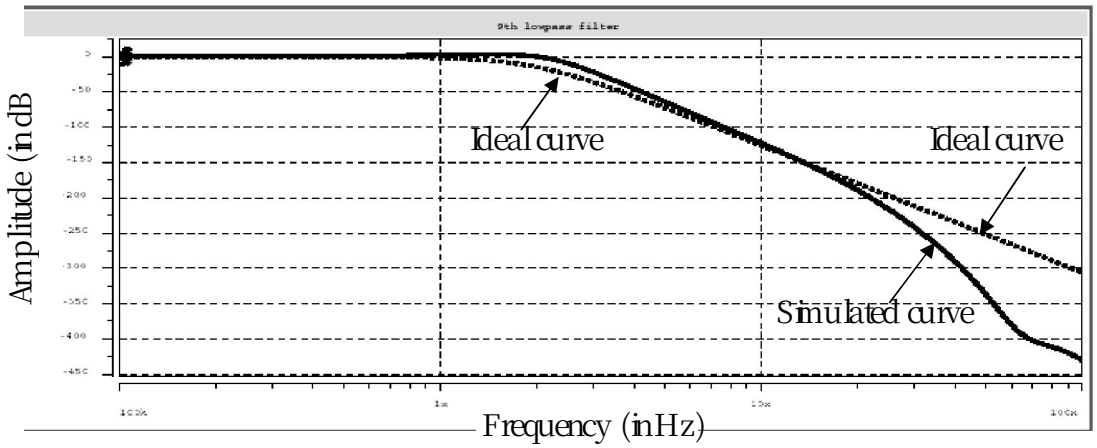


Fig. 14. The simulated frequency response of the ninth-order LV SRD LPF.

Conclusion

Based on the MOSFET square law, a systematic synthesis method for high-order square-root domain filter with reduced voltage is presented in this paper. This work is based on the MOSFET square law. Emphases are given on synthesizing filters. The keys to this work are the constructive settings of DC components for input signals, the DC voltages of the state-space variables, and the DC bias current I_0. The proposed prototypical circuits of low-voltage square-root domain filters are able to overcome the possible inequality of DC level between the input and output node. It is a significant and necessary improvement for the convenient and reliability of high-order filter realization since the inequality of input and output node of DC voltage will induce the incomplete power propagation and seriously degrade the frequency response of the filter. Moreover, by means of adjusting the range of the DC bias current I_0 in the acceptable boundary, which may be established and attainable during the process of designing for the proposed prototypical circuits of SRD filters, it provides that the center frequency f_0 or 3 dB frequency f_{3dB} are not only attainable at megahertz frequencies but also tunable electronically. Simulations for the proposed high-order LV SRD filters, based on 0.25μm CMOS process and operated with 1.5 V power supply voltage, were provided and discussed throughout this paper. Simulated results, which indicate that the average errors of frequency response are less than 1.0%, demonstrate the validity of the proposed synthetic technique and the high performances of the proposed prototypical circuits of LV SRD filters. Hence, the proposed synthetic technique provides an alternative for performing high-order square-root domain filter implemented by standard digital CMOS technology.

References

1. Adams RW. Filtering in the log-domain. 63rd AES Conf, New York, 1979, 1470.
2. Frey DR. Log-domain filtering: an approach to current-mode filtering. IEE Proc. Pt. G, 1993;140 (12):406-416.
3. Frey DR. Exponential state space filters: A generic current-mode design strategy. IEEE Trans. Circuits Syst. I, 1996;43(1): 34-42.
4. Tsividis Y. Externally linear, time-invariant systems and their application to companding signal processors. IEEE Trans. Circuits Syst. II, 1997;44(2): 65–85.
5. Drakakis EM, Payne AJ, Toumazou C. Log-domain state-space: a systematic transistor-level approach for log-domain filtering. IEEE Trans. Circuits Syst. II, 1999;46(3):290-305.
6. Drakakis EM, Payne AJ, Toumazou C. Log-domain filters, translinear circuits and the Bernoulli cell. IEEE ISCAS, Hong Kong, 1997;1:501–504.
7. Drakakis EM, Payne AJ, Toumazou C. Log-domain filtering and Bernoulli cell. IEEE Trans. Circuits Syst. I, 1999;46(5):559-571.
8. Toumazou C, Ngarmnil J, Lande TS. Micropower log-domain filter for electronic cochlea. Electron. Lett, 1994; 30(10):1839–1841.
9. Germanovix W, O'neill G, Toumazou C, *et al.* Analogue micropowered log-domain tone controller for auditory prostheses. Electron. Lett, 1998;34(11):1051-1052.
10. Eskiyerli MH, Payne AJ, Toumazou C.

State-space synthesis of biquads based on the MOSFET square law. IEEE Int. Symp. Circuits and Syst, 1996;1: 321-324.
11. Yu GJ, Liu BD, Hsu YC, *et al.* 'Design of log domain low-pass filters by MOSFET square law,' in Proc. The Second IEEE Asia Pacific Conf. on ASICs, 2000; 9-12.
12. Yu GJ, Huang CY, Chen JJ, *et al.* Design of Square-Root Domain Filters. Analog Integrated Circuits and Signal Processing, (Accepted), 2004.
13. Lopez-Martin AJ, Carlosena A. A 3.3V tunable current-mode square-root domain biquad. IEEE Int. Symp. On Circuits and Systems, 2000;5-8.
14. Eskiyerli MH, Payne AJ, Tournazou C. State-space synthesis of integrators based on the MOSFET square law. Electron. Lett, 1996;32(6):505-506.
15. Mulder J, van der Woerd AC, Serdijn WA, *et al.* Current-mode companding √x-domain integrator. Electronics Lett, 1996;32(3):198-199.
16. Mulder J, van der Woerd AC, Serdijn WA, *et al.* A 3.3 V current-controlled √x-domain Oscillator. Analog Integrated Circuits and Signal Processing, 1998;16(1):17-28.
17. Eskiyerli MH, Payne AJ, Square-root domain filter design and performance. Analog Integrated Circuits and Signal Processing, 2000;22(2-3):231-243.
18. Lopez-Martin AJ, Carlosena A. Systematic design of companding systems by component substitution. Analog Integrated Circuits and Signal Processing, 2001;28(3):91-106.
19. Lopez-Martin AJ, Carlosena A. Current-Mode Multiplier-Divider Circuits Based on the MOS Translinear Principle. Analog Integrated Circuits and Signal Processing. 2001;28(3):265-278.
20. Steyaert M, Crols J, Gogaert S, *et al.* Low-voltage analog CMOS filter design. IEEE Int. Symp. On Circuits and Systems, ISCAS '93, 1993;2: 1447-1450.
21. Rajput SS, Jamuar SS. Low voltage, low power, high performance current mirror for portable analogue and mixed mode applications. IEE Proc. Circuits, Devices and Systems, 2001;148: 273-278.
22. Ramirez-Angulo J, Carvajal RG, Torralba A, *et al.* The flipped voltage follower: a useful cell for low-voltage low-power circuit design. IEEE Int. Symp. On Circuits and Systems, ISCAS 2002, 2002;3:615-618.
23. Mulder J, Van der Woerd AC, Serdijn WA, *et al.* High-swing cascode MOS current mirror. Electronics Lett, 1996;32(14):1251 – 1252.
24. Zeki A, Kuntman H. Accurate and high output impedance current mirror suitable for CMOS current output stages. Electronics Lett, 1997;33(12):1042-1043.
25. Blalock BJ, Allen PE, Rincon-Mora GA, Designing 1-V op amps using standard digital CMOS technology. IEEE Trans. Circuits and Systems II, 1998;45(7):769-780.
26. Heim P, Jabri MA. MOS cascode-mirror biasing circuit operating at any current level with minimal output saturation voltage. Electronics Lett, 1995;31(9):690 – 691.
27. Prodanov V I, Green MM. CMOS current mirrors with reduced input and output voltage requirements. Electronics Lett, 1996;32(2):104 – 105.
28. Itakura T, Czamul Z. High output-resistance CMOS current mirrors for low- voltage applications. IEICE Trans 1997; E80-A (1):230-232.
29. Lopez-Martin AJ, Carlosena A. A 1.5 V CMOS square-root domain filter. IEEE Int. Conf. On Electronics, Circuits and Systems, 2001;1465-1468.
30. Lopez-Martin AJ, Carlosena A. A 1.5 V CMOS companding filter,' Electron. Lett, 2002;38(10): 1346-1348.
31. Yu GJ, Chen JJ, Lin HY, *et al.* A low-voltage low-power log-domain band-pass filter. IEEE Int. Symp. On VLSI Technology, Systems, and Applications, 2003;219-222.
32. Yu GJ, Huang CY, Chen JJ, *et al.* Design of Current-Mode Square-Root Domain Band-Pass Filter with Reduced Voltage. Analog Integrated Circuits and Signal Processing, (Accepted), 2004.
33. Chen CT. Linear system theory and design. (CBS College Publishing, Holt, Rinehart & Winston, New York, 1984).
34. Sinha NK. Control Systems. (CBS College Publishing, Holt, Rinehart & Winston, New York, 1986).
35. Nise Norman S. Control Systems Engineering. (John Wiley & Sons, Inc., New York, 2000).