1V Square-Root Domain Low-Pass Filter using Translinear Loop Technology in Biomedical Engineering

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Abstract A low voltage square root domain filter based on the MOSFET square law is proposed in this report. Through the verification of HSPICE simulation, the extendibility and the reliability of the design procedure are proved. Furthermore, the voltage supply is successfully leveled down to 1V by the level shifter low-voltage technique without regarding the performance of the filters. The proposed filter structure has the merits of low-power voltage supply operation, high frequency operation, and the wide range of pole frequency tuning ability. The proposed circuit has been fabricated with TSMC 0.35 μm CMOS technology. The experimental results have verified the center frequency f3dB of the low-pass filter can be electronically tunable in the range of 0.4 MHz to 2.9 MHz. The total harmonic distortion (THD) is less than 0.7% for signal amplitude of 100 mV, and the power dissipation is less than 1.05 mW. [Life Science Journal. 2009; 6(4): 92–96] (ISSN: 1097 – 8135)

Key Words square-root domain , translinear Loop, low-Pass Filter, square-root domain filter, flipped-voltage follower

1 Introduction

Recently, there is a growing interest in the field of translinear filters. Main advantages of these various filters are regarding to large dynamic range and low-voltage/low power operation capability. Since the voltage swings of the internal capacitors are compressed, the dc power supply voltage will be less restrictive to the maximum input signal. Initially, a subclass of translinear filters is log-domain filters introduced by Adams [1]. On the other hand, a subclass of translinear filters, named "square-root domain filter" was introduced. Toumazou [2] proposed the state-space synthesis of the second filter which is the first filter structure using the MOSFET square law. Although an alternative biasing of MOS translinear loops based on the application of the Flipped-Voltage Follower (FVF) is proposed [3-5], it allows to significantly reduce the voltage supply requirements. In order to improve the problem of Germanovix'a [6] method, Psychalinos [7], Yu [8] and Lopez-Martin [9-10] also adopted MOSFETs operated in saturation region to implement the square-root domain filters. In this paper, a square-root domain filter with voltage supply down to 1V has been proposed. The paper is organized as follows: In Section II, the principle and architecture of the square-root domain filter using state-space approach is derived and explained. Then in Section III, the most supply-voltage critical block, i.e. the square-root circuit, which performs the geometric-mean function, is proposed to operate at a supply as low as 1V. By using the proposed circuit implementation as well as the state-space approach, several filter prototypes are designed for the verification of the proposed idea in Section IV. Finally, a brief conclusion is given at the end of this paper.

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. 2. Principle And Architecture

Consider the transfer function of the first-order low-pass filter (LPF):

$$H(S)=\frac{\omega_0}{s+\omega_0}=\frac{Y(S)}{U(S)} \quad (1)$$

where $Y(s)$ and $U(s)$ are output and input respectively, and the relationship between them is obtained by

$$Y(S)=\frac{\omega_0}{S+\omega_0} \tag{2}$$

Apply the inverse Laplace transform to (2), and then set the initial value to zero.

$$\dot{y}=-\omega_0 y+\omega_0 u \tag{3}$$

Let $y=x$ and take the derivative of both side.

$$\dot{y}=\dot{x} \tag{4}$$

According to the state-space approach, we could map the original transfer function into the stat-space equation.

$$\begin{cases}\dot{x}=-\omega_0 x+\omega_0 u\\ y=x\end{cases} \tag{5}$$

Assume the state variables are the node voltage, then $x=V_1$ and, $u=U$ and substitute them into (5).

$$\begin{cases}\dot{V}_1=-\omega_0 V_1+\omega_0 U\\ y=V_1\end{cases} \tag{6}$$

Multiply a constant C on both sides in (6).

$$\begin{cases}C\dot{V}_1=-C\omega_0 V_1+C\omega_0 U\\ y=V_1\end{cases} \tag{7}$$

The drain current of a MOSFET transistor operated in saturation can be expressed as

$$I_D=\frac{\mu_0 C_{OX} W}{2L}(V_{GS}-V_T)^2\equiv\beta(V_{GS}-V_T)^2 \tag{8}$$

where β, V_{GS} and V_T are the transconductance parameter, the gate-to-source voltage and the threshold voltage, respectively. Next, we define two new current variables I_1 and I_U to be

$$\begin{cases}I_1=\beta(V_1-V_T)^2\Rightarrow V_1=\sqrt{\frac{I_1}{\beta}}+V_T\\ I_U=\beta(U-V_T)^2\Rightarrow U=\sqrt{\frac{I_U}{\beta}}+V_T\end{cases} \tag{9}$$

And substitute the (9) into (7)

$$\begin{cases}C\dot{V}_1=C\omega_0\left(\sqrt{\frac{I_U}{\beta}}-\sqrt{\frac{I_1}{\beta}}\right)\\ y=V_1\end{cases} \tag{10}$$

Induce a new current variable here, and we know that the pole frequency ω_0 can be tuned by changing the DC current bias current source I_0.

$$I_0=\frac{C^2{\omega_0}^2}{\beta} \tag{11}$$

or

$$\omega_0=\frac{\sqrt{I_0\beta}}{C} \tag{12}$$

Thus, the state- space equation become

$$\begin{cases}C\dot{V}_1=\sqrt{I_0 I_U}-\sqrt{I_0 I_1}\\ y=V_1\end{cases} \tag{13}$$

The transfer function of a second-order low-pass filter can be expressed as

$$H(s)=\frac{\omega_0^2}{s^2+\left(\frac{\omega_0}{Q}\right)s+\omega_0^2} \tag{14}$$

This transfer function of a low-pass filter can be expressed as

$$\begin{cases}\dot{x}_1=-\omega_0 x_2+\omega_0 u\\ \dot{x}_2=\omega_0 x_1-\left(\frac{\omega_0}{Q}\right)x_2\\ y=x_2\end{cases} \tag{15}$$

Where x_1, x_2, y, and u are state variables, output and input signals, respectively. If the node voltages V_1 and V_2 are assumed to be the state variables, x_1 and x_2, and a voltage signal U denotes the input u, the Eq.(15) can be rewritten as

$$\begin{cases}C\dot{V}_1=-C\omega_0 V_2+C\omega_0 U\\ C\dot{V}_2=C\omega_0 V_1-\left(\frac{C\omega_0}{Q}\right)V_2\\ y=V_2\end{cases} \tag{16}$$

Where C is a multiply factors. $C\dot{V}_1$ and $C\dot{V}_2$ in Eq.(16) can be regarded as the time-dependent current through

the two capacitors C connected from V_1 to ground and from V_2 to ground, respectively.

The drain current of a MOSFET transistor operated in saturation can be expressed as

$$I_D = \frac{\mu_0 C_{ox} W}{2L}\left(V_{GS} - V_{th}\right)^2 = \beta\left(V_{GS} - V_{th}\right)^2 \quad (17)$$

Where β, V_{GS} and V_{th} are the device trans-conductance parameter, the gate-to-source voltage and the threshold voltage, respectively. thus, the state-space equation becomes

$$\begin{cases} C\dot{V}_1 = \sqrt{I_0 I_U} - \sqrt{I_0 I_2} \\ C\dot{V}_2 = \sqrt{I_0 I_1} - \dfrac{\sqrt{I_0 I_2}}{Q} \end{cases} \quad (18)$$

According to Eq. (17), and supposing Q=1, the state equations in Eq. (16) can be written as

$$\begin{cases} C\dot{V}_1 = \sqrt{I_0 I_U} - \sqrt{I_0 I_2} \\ C\dot{V}_2 = \sqrt{I_0 I_1} - \sqrt{I_0 I_2} \end{cases} \quad (19)$$

where

$$I_1 = \beta(V_1 - V_T)^2 \quad (20)$$

$$I_2 = \beta(V_2 - V_T)^2 \quad (21)$$

$$I_U = \beta(U - V_T)^2 \quad (22)$$

and

$$\omega_0 = \frac{\sqrt{\beta I_0}}{C} \quad (23)$$

$$I_0 = \frac{C^2 {\omega_0}^2}{\beta} \quad (24)$$

Note that ω_0 is inversely proportional to the capacitance C and is proportional to the square root of I_0; hence the cutoff frequency ω_0 is dominated by the capacitance C and I_0 is used to tune the cutoff frequency.

3. Circuit Implementation

3.1 Current-mode Flipped-Voltage Follower circuit

Fig. 1 [3-5] shows a flipped voltage follower (*FVF*), which consists of a current source and two transistors. One transistor is cascaded another. The current source supplies the drain current of M_1, and the drain of M_1 connects to the gate of M_2 can be expressed as

$$V_{io} \equiv V_x + V_{th}$$
$$V_x = \sqrt{\frac{I_B}{\beta}} \quad (25)$$

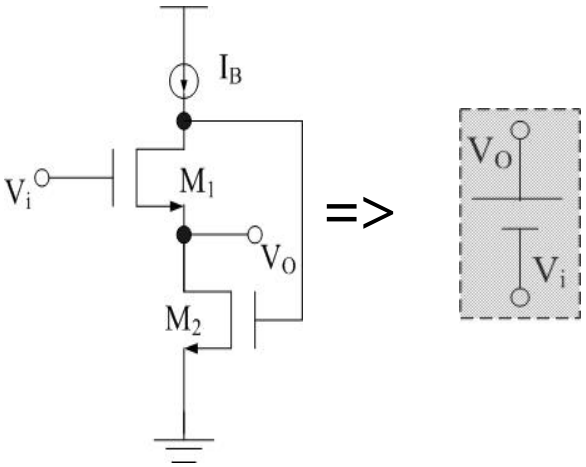

Fig 1. Current-mode Flipped-Voltage Follower (*FVF*) circuit

3.2 Current-mode square-root circuit

The proposed current-mode square-root circuit is shown in Fig. 2 operating as follows: Ix and Iy are input currents, and these currents generate the corresponding voltage, VX and VY through the current to voltage conversion of diode-connected MOS. The matched transistors M1-M4 which is forced to operate in subthreshold region and the dc current sources, depicted as Ib altogether construct a voltage-averaging circuit.

The voltage averaging circuit produces a gate voltage VXY , which is forced to be equal to the average of the gate voltage of MX and MY as VXY = (VX+VY)/2. The detailed circuit operation of averaging function is explained as follows: As we know, the I-V relationship between the drain current and gate-source voltage for a MOS operated in subthreshold region can formulated as the following equation:

$$I_D = I_{D0} \exp\left(\frac{V_{GS}}{\xi V_{th}}\right) \quad (26)$$

where ξ and VT stand for non-ideal factors and thermal voltage respectively. We can easily find the following equation holds since ID1+ID2=ID2+ID3= Ib

$$I_{D3} = I_{D1} \quad (27)$$

Substitute Eq.(26) into Eq.(27) , the equation can be rewritten as

$$I_{D0}\exp\left(\frac{V_{S2}-V_X}{\xi V_{th}}\right)=I_{D0}\exp\left(\frac{V_{S3}-V_{XY}}{\xi V_{th}}\right) \tag{28}$$

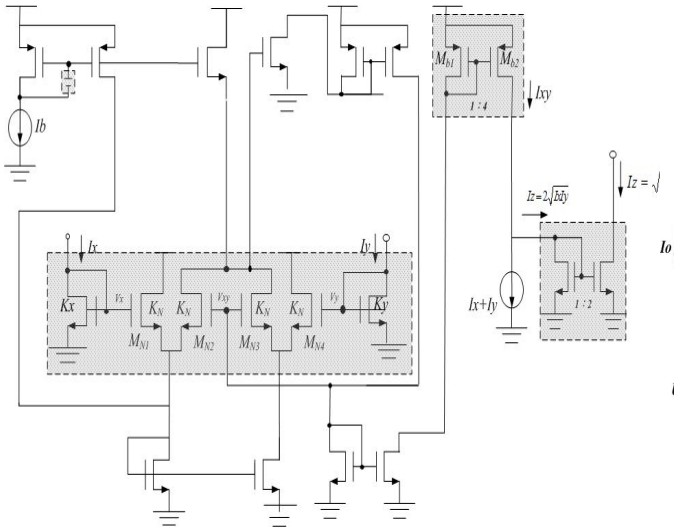

Fig. 2. Current-mode square-root circuit (a) Circuit diagram, (b) Equivalent block diagram

From Eq.(27) we can derive the result :

$$V_{XY}=V_{S3}-V_{S1}+V_X \tag{29}$$

In the similar way, we can get the following result by the same analysis procedure.

$$V_{XY}=V_{S1}-V_{S3}+V_Y \tag{30}$$

According to Eq.(29) and Eq.(30), we can prove the following Eq.(31).

$$V_{XY}=\frac{V_X+V_Y}{2} \tag{31}$$

According to the translinear loop formed by transistors MX, MY, and MXY, realized under the assumption that βb12 = 4β and βx = βy = β where β is the aspect ratio, the following equation can be derived.

$$I_{xy}=I_x+I_y+2\sqrt{I_xI_y} \tag{32}$$

Again writing the KCL equation at output node of this circuit, the equation can be inducted as follows:

$$I_z=2\sqrt{I_xI_y} \tag{33}$$

Hence if the ratio of the output stage current mirror in Fig. 2 is set to be 2:1, the output current Iout can be derived as:

$$I_{out}=\sqrt{I_xI_y} \tag{34}$$

The circuit diagram of second-order low-pass filter is shown in Fig. 3.

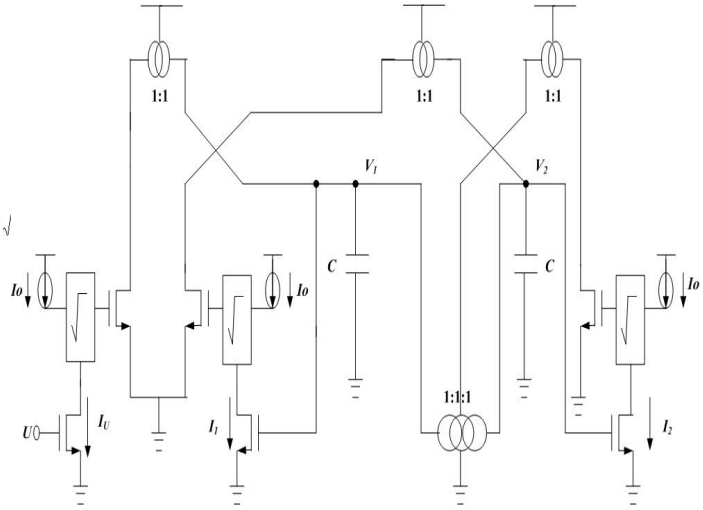

Fig. 3. Circuit diagram of the second-order low-pass filter

4. Simulation Results

Fig. 4 is the simulated result of the current-mode square-root circuit while VDD = 1V, Ix and Iy are a 40 μA DC current and a triangle wave current with values between 0 and 45 μA, respectively. Fig. 5 is the frequency f3dB tuning range of second-order low-pass filter shown in Fig. 3 which is from 0.420MHz, 0.779MHz and 1.12 MHz by changing the current I0 from 20uA, 30uA and 40uA. The total harmonic distortion (THD) with a 1KHZ 100mV peak-to-peak sinusoid is 0.681%. The specifications of second-order low-pass filter are shown in Table 1.

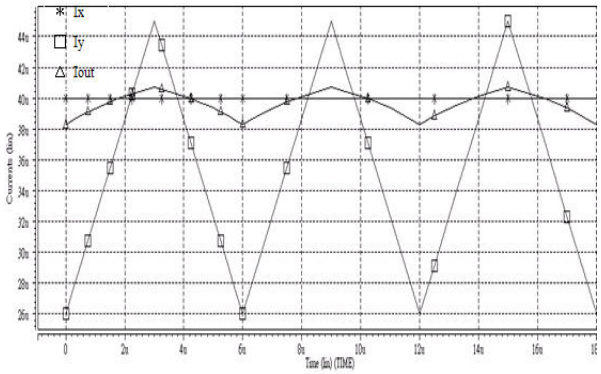

Fig. 4 Simulated result of the square-root circuit

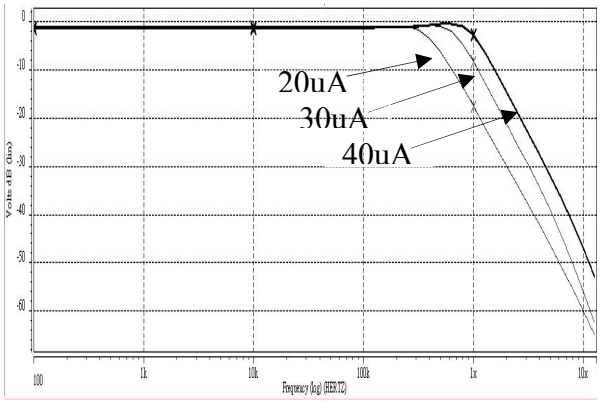

Fig 5 Frequency response of the second-order low-pass filter.

5. Conclusion

In this paper, based on the MOSFET square law, on square-root domain low-pass filters with low voltage and low power operation is proposed. Operated in 1V power supply voltage, low-pass filter has been fabricated in 0.35μm CMOS technology; shown that the center frequency f0 is not only attainable at megahertz frequencies but also tunable electronically. The proposed circuit, thus, has the advantages of high frequency operation, low supply voltage operation and low power consumption. Furthermore, implementation via standard digital CMOS technology for the proposed filter is quite suitable for system-on-a-chip (SOC) application.

Table 1. Specifications of the second-order low-pass filter

Parameters	Simulation results
Filter order	2
Technology	TSMC 0.35 μm
Supply voltage	1V
I_0	20uA, 30uA, 40uA
f_{3db} tuning range	0.420 MHz, 0.779 MHz, 1.12 MHz
power dissipation	0.599mW, 0.864mW, 1.035mW
THD (V_{PP}=0.1V)	0.872%, 0.696%, 0.681%

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