On the realization of floating inductors

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Abstract: Floating inductor circuits using minimum number of passive elements namely two resistors and one capacitor is reviewed in this paper. All the circuits considered in this paper are floating. Previously reported non-floating circuits are modified to be floating and new floating circuits are introduced as well. The active elements used in this paper are floating conveyor building blocks as well as pairs of non-floating conveyor blocks acting as a floating pair.
Simulation results of second order lowpass filters realized using different types of floating inductors are included.

Keywords: Floating inductors, current conveyors, gyrator, DVCC, FDVCC

1. Introduction

The classification of active RC circuits simulating floating inductors was given in [1]. The floating inductor circuits reported in [1] employ the operational amplifier (Op Amp) or the nullor element [2] known also as the operational floating amplifier (OFA) [3] as the active building block. Detailed derivation of the admittance matrix equation of different types of gyrators was given in [1]. A single Op Amp gyrator realization was introduced in [4]. Gyrator realization using two second generation current conveyors (CCII) with opposite Z polarities was introduced in [5].The use of single CCII- in realizing non-ideal inductor was first introduced in [6] followed by a single CCII+ gyrator circuit [7].
Simulated ideal floating inductors using CCII and transconductance amplifiers (TA) was classified and reviewed in [8] and new CCII floating gyrator circuits were given.
Most recently generation method of floating ideal inductors based on using nodal admittance matrix (NAM) expansion [9-10] was introduced in [11]. This paper concentrates on the realization of floating inductors using floating gyrator circuits and a single capacitor. The total number of resistors in each of the gyrator circuits considered is limited to two resistors.

2. Generalized Inductor Configurations

Figure 1(a) and (b) represent the two generalized configuration for floating inductor realization in accordance with the classification given in [1, 8]. The circuit shown in Figure 1(a) includes two general cases depending on the summation of the four currents.
If the summation $I_1 + I_2 + I_3 + I_4$ is not zero the circuit is not floating. On the other hand a necessary condition that the circuit is floating is given by [1, 8]:

$$I_1 + I_2 + I_3 + I_4 = 0 \tag{1}$$

Most of the floating inductor circuits that belong to the generalized configuration shown in Figure 1(a) in which the capacitor is grounded are not floating. Table III in [8] includes nine gyrator circuits that belong to this case.
Six generalized configurations that belong to type 1 are given in this paper. Eight generalized configurations that belong to type 2 are also given in this paper.
The first active building block that is used in the paper is the generalized conveyor (GC) defined by the following matrix equation:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ a & 0 & 0 \\ 0 & K & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{2}$$

The parameter a determines the type of conveyor, a CCII is realized if $a = 1$ and ICCII is obtained if $a = -1$.
The parameter K determines the conveyor Z polarity, for Z+ the parameter $K = 1$ and for Z– the parameter $K = -1$.
The GC includes four different types; the CCII– and the ICCII– are floating whereas the CCII+ and ICCII+ are not floating. The CCII+ and ICCII+ although non-floating can also be used in realizing floating circuits provided they are used in pairs as will be demonstrated in the next section.
Table 1 includes a summary of the floating conveyor building blocks that will be used in this paper.

3. Type I Inductor Circuits

In this section six floating circuits realizing floating inductors and using two resistors and one capacitor are considered.

3.1. Four Generalized Conveyor Circuit

The configuration shown in Figure 2 using four nullors was first reported in [1]. The generalized configuration using four CCII+ realized from operational amplifiers (Op Amps) together with current mirrors was first reported in [14] and republished in [15] with a comment given in [16]. The generalized configuration using four CCII– (equivalent to four nullors) was reported in [8]. The same generalized configuration using four ICCII– was reported in [17].

The circuit shown in Figure 2 employs four GC and a necessary condition for V_1 and V_2 to appear in a subtraction form is that $a_1 = a_2$. A necessary condition for the circuit to be floating is that $K_1 = K_2$.These two conditions imply that GC1 and GC2 must be matched.

A necessary condition for the current I_1 to equal to $-I_2$ is that $K_3 = K_4$. Although a_3 can be either 1 or –1 and has no effect on circuit operation it is taken equal to a_4 for a symmetrical circuit. Therefore GC3 and GC4 are taken to be matched.

By direct analysis it can be shown that:

$$I1= -I2 = \frac{V1-V2}{sCR1R2}\,[a1K1a4K4] \qquad (3)$$

A necessary condition for a floating inductor realization is that $a_1K_1a_4K_4$ must be +1. Eight possible conveyor realizations are given in Table II that satisfies this coefficient condition. It is seen that this approach of analysis resulted in five new conveyor circuits.

3.2 DVCC– and Two CCII– (ICCII–) Circuits

The circuit shown in Figure 3(a) is a modified version of the newly reported DVCC and two CCII+ circuit shown in Figure 14 of [11] by replacing the two CCII+ by two CCII– .The circuit is floating since I_G is zero and it realizes a floating inductor given by CR_1R_2.

Figure 3(b) represents a second equivalent floating circuit which uses two ICCII– instead of the two CCII– in Figure 3(a).

3.3 Two Floating DVCC Circuits

The two floating circuits shown in Figure 4 are new and they are obtained from the newly reported circuit shown in Figure 16 of [11]. The circuits employ the DVCC– and the newly defined floating DVCC (FDVCC) given in Table 1.

The third circuit is shown in Figure 5 is a modified version of the floating inductor circuit proposed in [20] by using the FDVCC instead of the DVCC+ in [20].

The three circuits shown in Figures 4 and 5 are floating since I_G is zero and each realizes a floating inductor given by CR_1R_2.

4. Type II Inductor Circuits

The circuit shown in Figure 6(a) is a modified version of Figure 2. It was introduced in [1] using four nullors and in [19] using four CCII– or four CCII+, it was also reported in [8] using four CCII–. The GC1 and GC2 must be identical types; also GC3 and GC4 must be identical types. The types of conveyors given in Table II apply to this floating circuit also.
An alternative generalized configuration realizing a floating inductor is shown in Figure 6(b). The GC1 and GC2 must be identical types; also GC3 and GC4 must be identical types. By direct analysis it can be shown that:

$$I1 = -I2 = -\frac{V1 - V2}{sCR1R2}\,[a_1K_1a_3K_3] \qquad (4)$$

A necessary condition for a floating inductor realization is that $a_1K_1a_3K_3$ must be -1. Eight possible conveyors realizations are given in Table III that satisfies this coefficient condition. It is seen that seven new circuits are generated based on this circuit topology.
Figure 7(a) represents a floating inductor circuit using two CCII+ and one CCII– [20]. This is among the four floating gyrator circuits reported in [8]. A modified floating inductor circuit using two ICCII– and one CCII–is shown in Figure 7(b).
Figure 8(a) represents a modified floating inductor circuit to the two DVCC circuit reported in [21] using two FDVCC in order to have a floating circuit with I_G equal to zero. An alternative new equivalent circuit is shown in Figure 8(b). Both circuits realize an inductor of magnitude CR_1R_2.

5. Simulation Results

The CMOS circuit realizing the FDVCC is obtained directly from the well known DVCC [21] by adding the two MOS transistors M_{19} and M_{20} as shown in Figure 9.
The transistor aspect ratios are given in Table IV based on the 0.5µm CMOS model from MOSIS. The supply voltages used are ± 1.5 V and V_{B1}= –0.52 V and V_{B2} = 0.33 V.
This circuit will be used in the following simulations to realize different types of conveyors.
As an application of some of the floating circuits reported, a floating inductor of magnitude 0.253 m. H is realized the capacitor C =100pF;

$R_1 = R_2 = 1.59$ kΩ. The floating inductor is used to realize a maximally flat (Q=0.707) second order low-pass filter with cutoff frequency of 1MHz using a series resistor of $R_S = 2.25$ kΩ and C_S of 100pF.
Fig. 11(a) represents the simulated magnitude and phase responses together with the ideal responses using the inductor circuit of Figure 2 with four ICCII+.
Fig. 10(b) represents the simulated magnitude and phase responses together with the ideal responses using the inductor circuit of Figure 3(a).
Fig. 10(c) represents the simulated magnitude and phase responses together with the ideal responses using the inductor circuit of Figure 5.
Fig. 11(a) represents the simulated magnitude and phase responses together with the ideal responses using the inductor circuit of Figure 6(b) with four ICCII+.
Fig. 11(b) represents the simulated magnitude and phase responses together with the ideal responses using the inductor circuit of Figure 7(b).
Fig. 11(c) represents the simulated magnitude and phase responses together with the ideal responses using the inductor circuit of Figure 8(b).

6. Conclusions

Realization of ideal inductor circuits using different types of conveyor building blocks is reviewed. Two types of inductor circuits are defined as was originally classified in [1]. The FDVCC is defined and is used in several circuits in this paper. Spice simulation results are given. Although this paper is partially a review paper it includes several new floating circuits.

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Table 1 Floating building blocks used in the paper

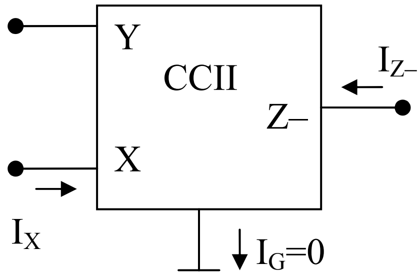
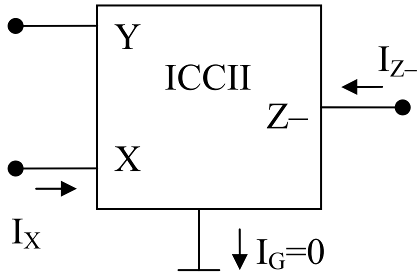
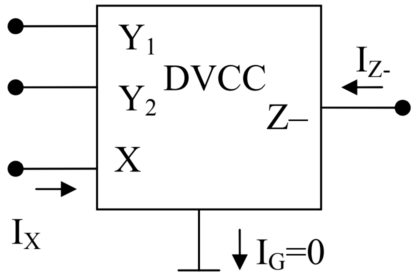
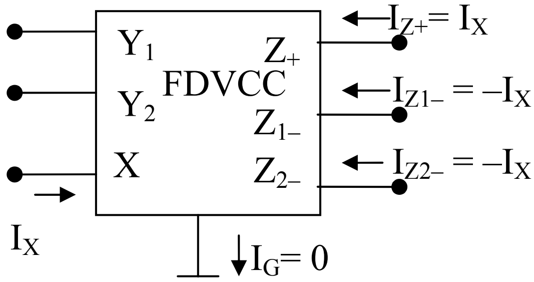
Conveyor	Definition	Floating Building Block Symbol
CCII- [5]	$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$	
ICCII-[12]	$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix}$	
DVCC- [13]	$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z-} \end{bmatrix}$	
FDVCC [New]	$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z+} \\ I_{Z1-} \\ I_{Z2-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z+} \\ V_{Z1-} \\ V_{Z2-} \end{bmatrix}$	

Table 2 Eight alternative conveyor circuits based on Figure 2

Circuit	a_1, a_2	K_1, K_2	a_3, a_4	K_3, K_4	GC_1,GC_2	GC_3,GC_4	Ref
1	+	+	+	+	CCII+	CCII+	14–16
2	+	–	+	–	CCII–	CCII–	1, 8
3	–	–	+	+	ICCII–	CCII+	New
4	+	+	–	–	CCII+	ICCII–	New
5	–	+	–	+	ICCII+	ICCII+	New
6	–	+	+	–	ICCII+	CCII–	New
7	+	–	–	+	CCII–	ICCII+	New
8	–	–	–	–	ICCII–	ICCII–	17

Table 3 Eight alternative conveyor circuits based on Fig. 6(b)

Circuit	a_1, a_2	K_1, K_2	a_3, a_4	K_3, K_4	GC_1,GC_2	GC_3,GC_4	Ref
1	+	–	+	+	CCII–	CCII+	8
2	+	+	+	–	CCII+	CCII–	New
3	–	+	+	+	ICCII+	CCII+	New
4	+	+	–	+	CCII+	ICCII+	New
5	+	–	–	–	CCII–	ICCII–	New
6	–	+	–	–	ICCII+	ICCII–	New
7	–	–	+	–	ICCII–	CCII–	New
8	–	–	–	+	ICCII–	ICCII+	New

Table 4 Transistor aspect ratios of the FDVCC of Fig.10

MOS Transistors	W(μm)/L(μm)
M_1, M_2, M_3,M_4	8/1
M_5 , M_6	8/1
M_{12}, M_{13}, M_{14}, M_{15}, M_{16}, M_{17}	20/2.5
M_7, M_8	10/1
M_9, M_{10}, M_{11}, M_{18}, M_{19}, M_{20}	40/2

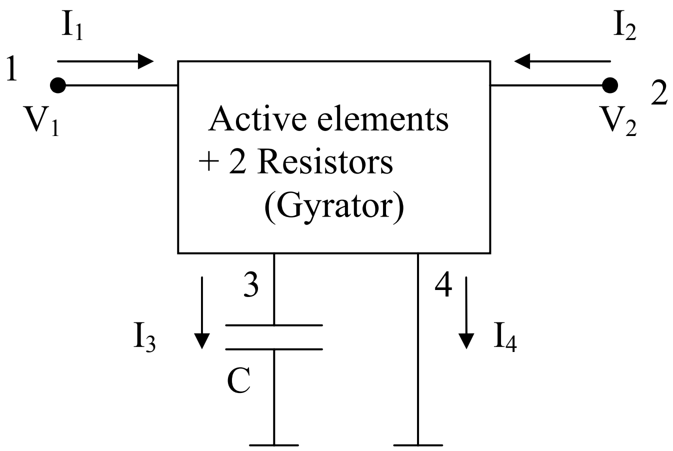


Figure 1(a) Generalized Type I configuration

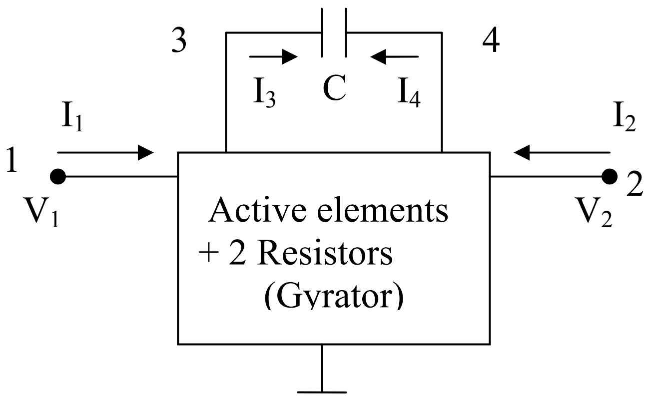


Figure 1(b) Generalized Type II configuration

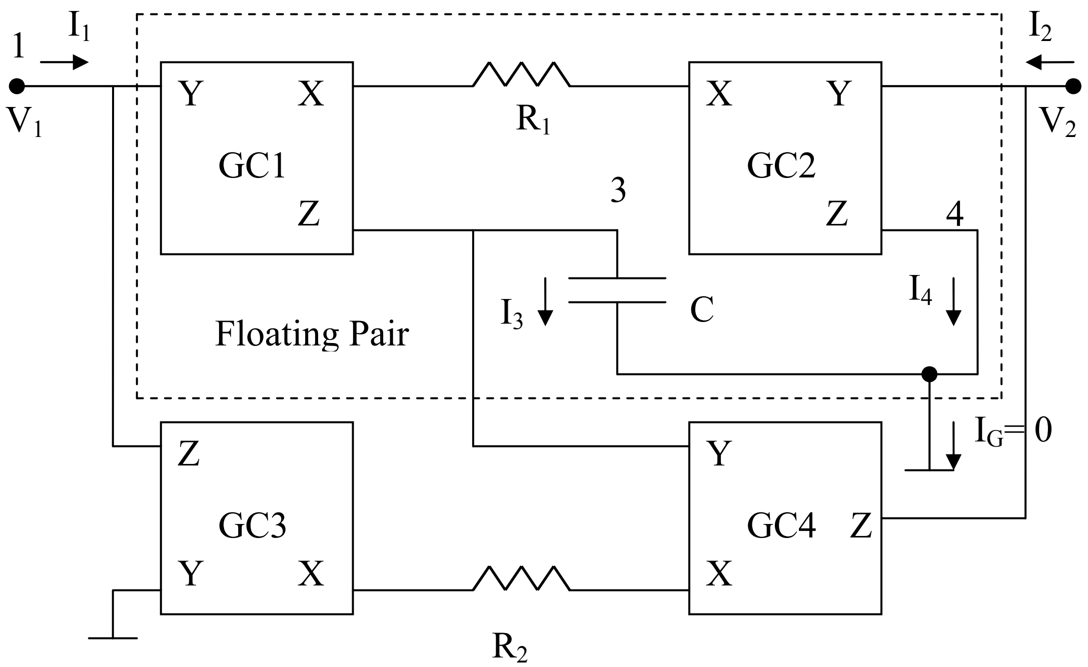


Figure 2 A floating inductor using four generalized conveyor

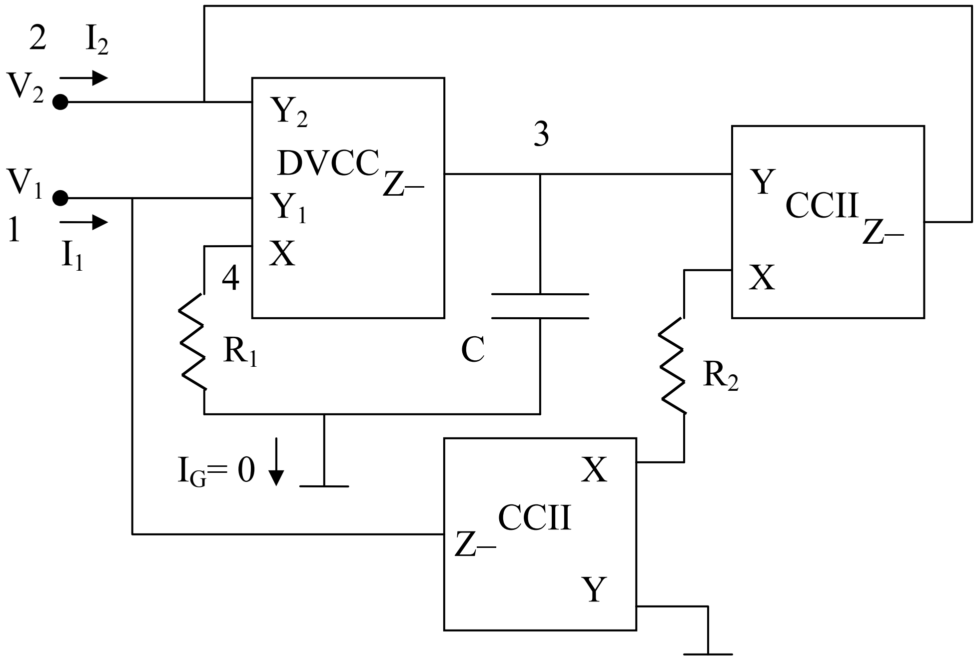


Figure 3(a) A floating inductor using a DVCC and two CCII- [11]

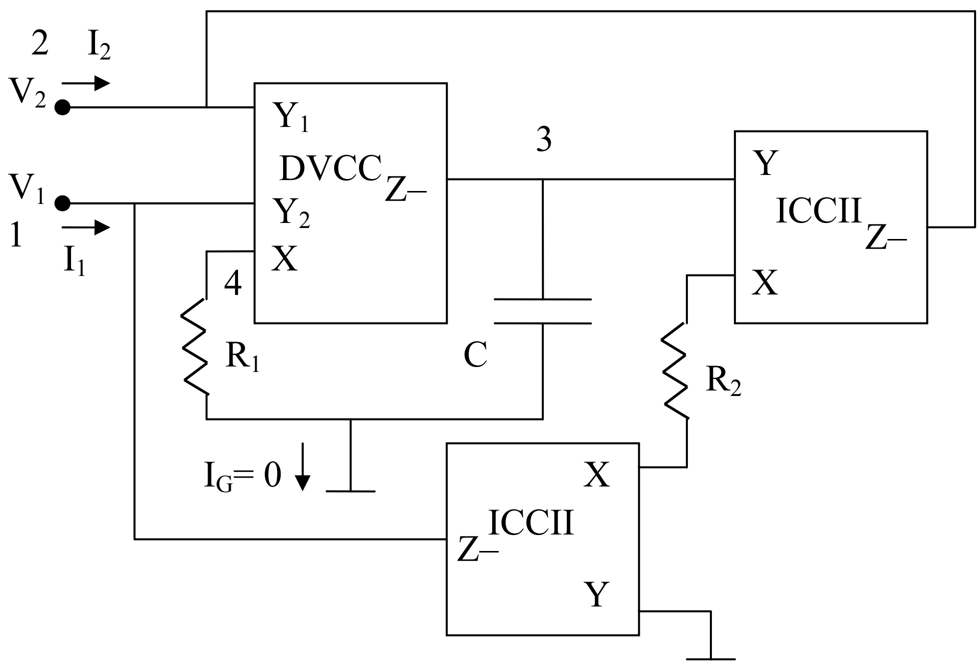


Figure 3(b) Alternative floating inductor using a DVCC and two CCII-

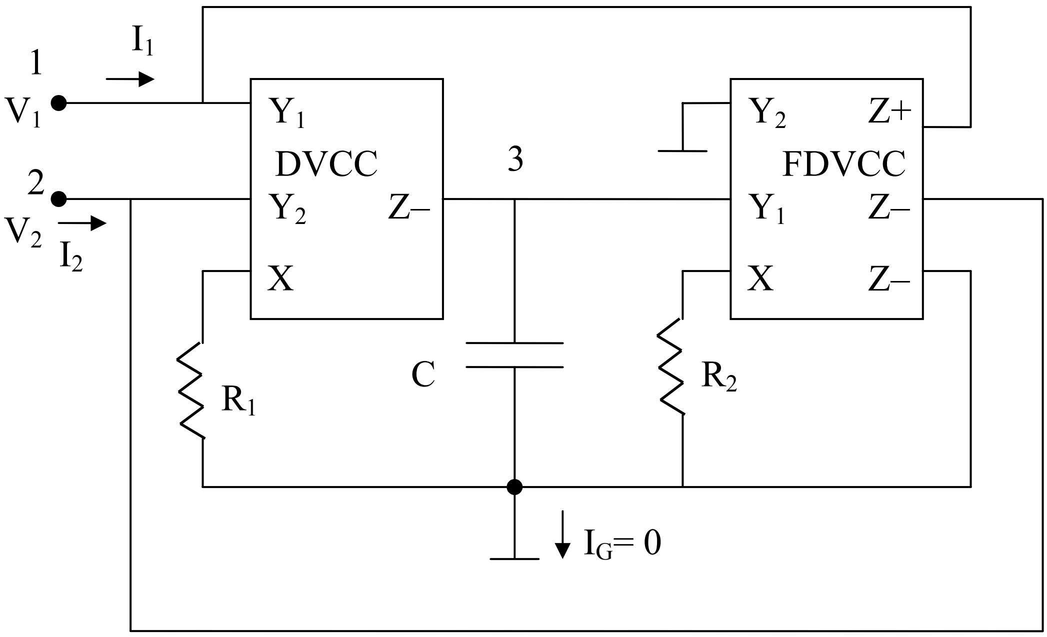
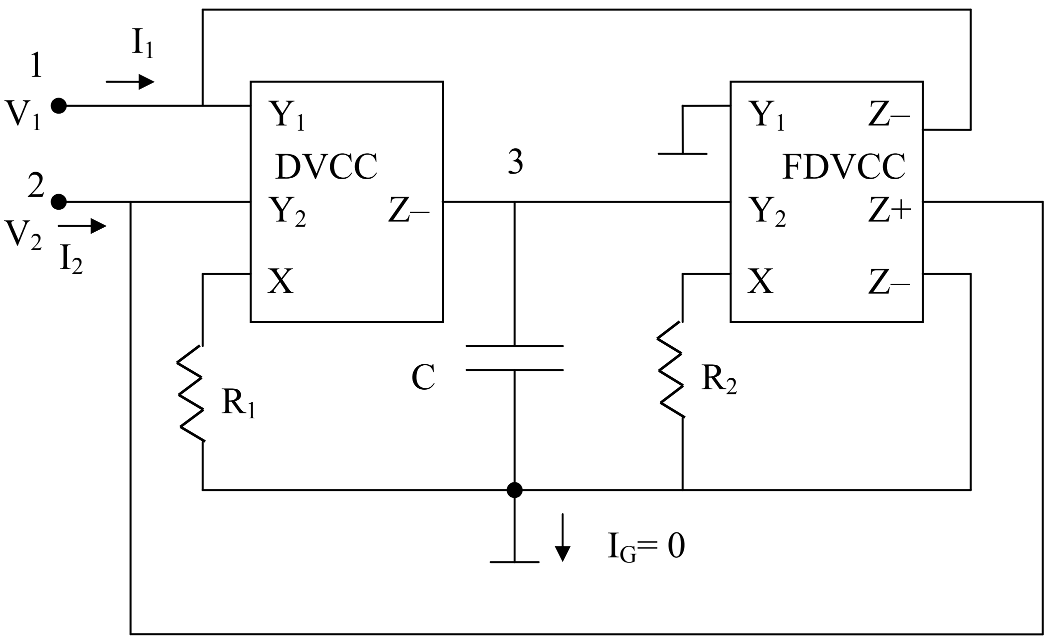


Figure 4(a)



4(b)

Figure 4 Two floating inductor circuits using DVCC and FDVCC [11]

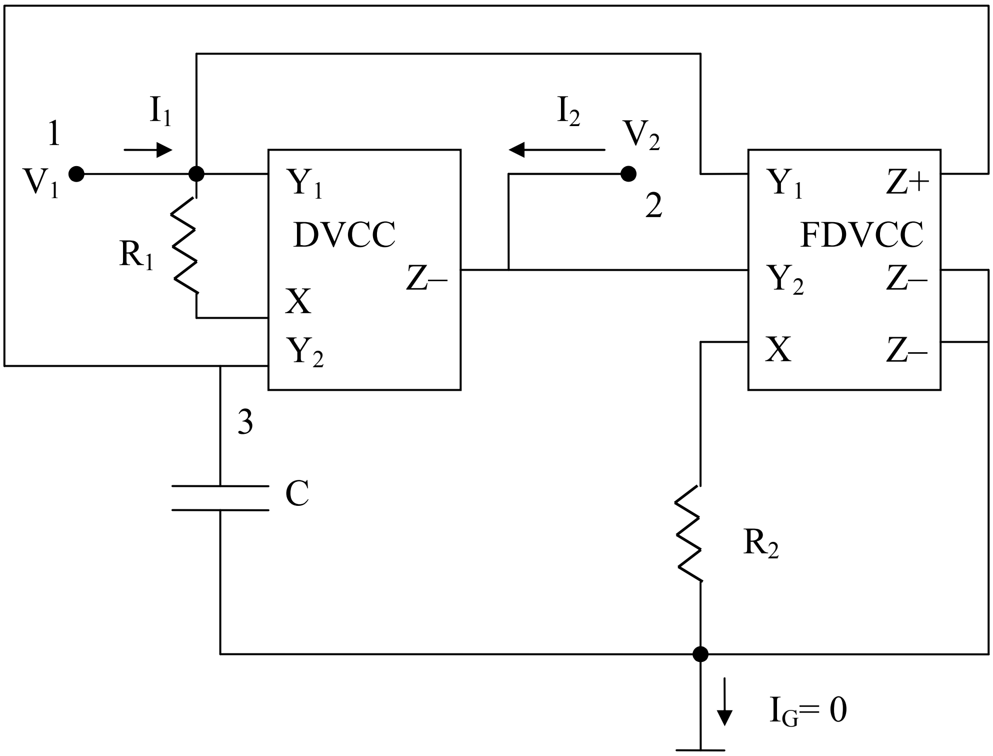


Figure 5 A modified floating inductor using DVCC and FDVCC [18]

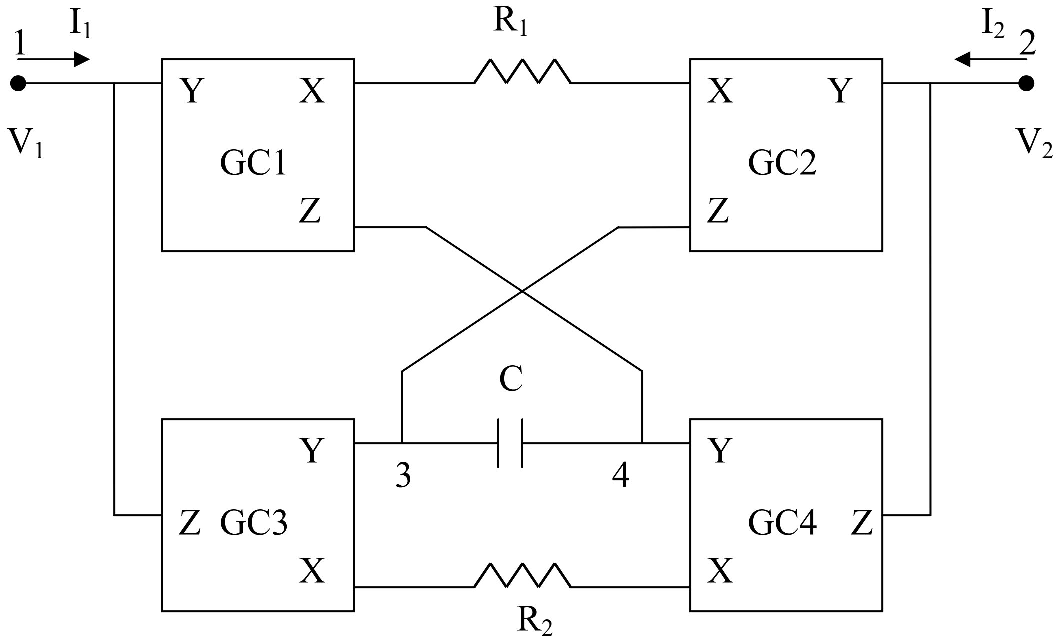


Figure 6(a) A floating inductor using four generalized conveyors [19]

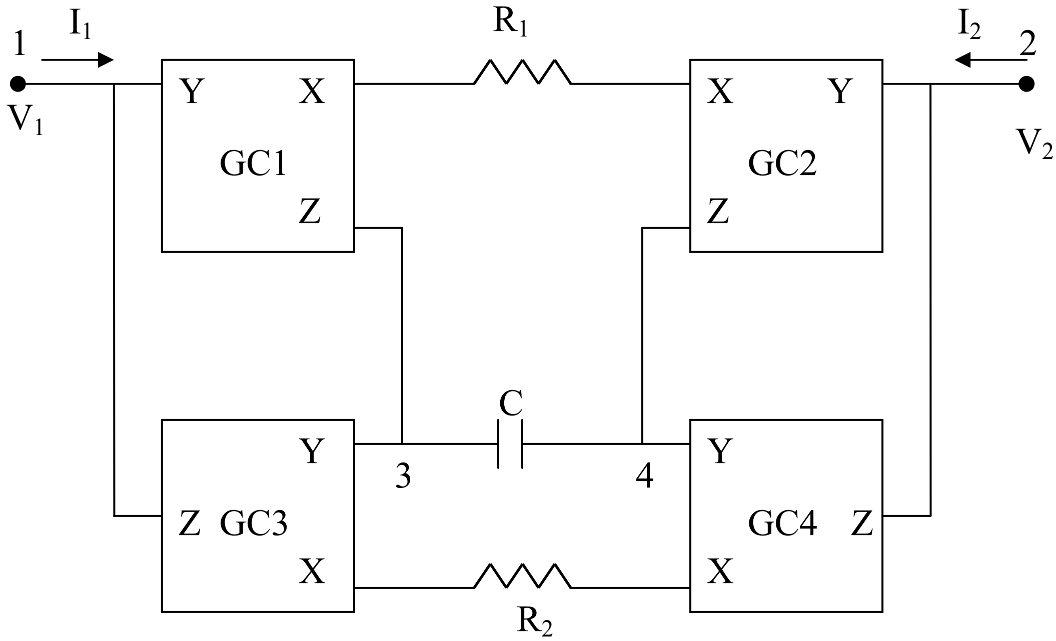


Figure 6(b) Alternative floating inductor using four generalized conveyors

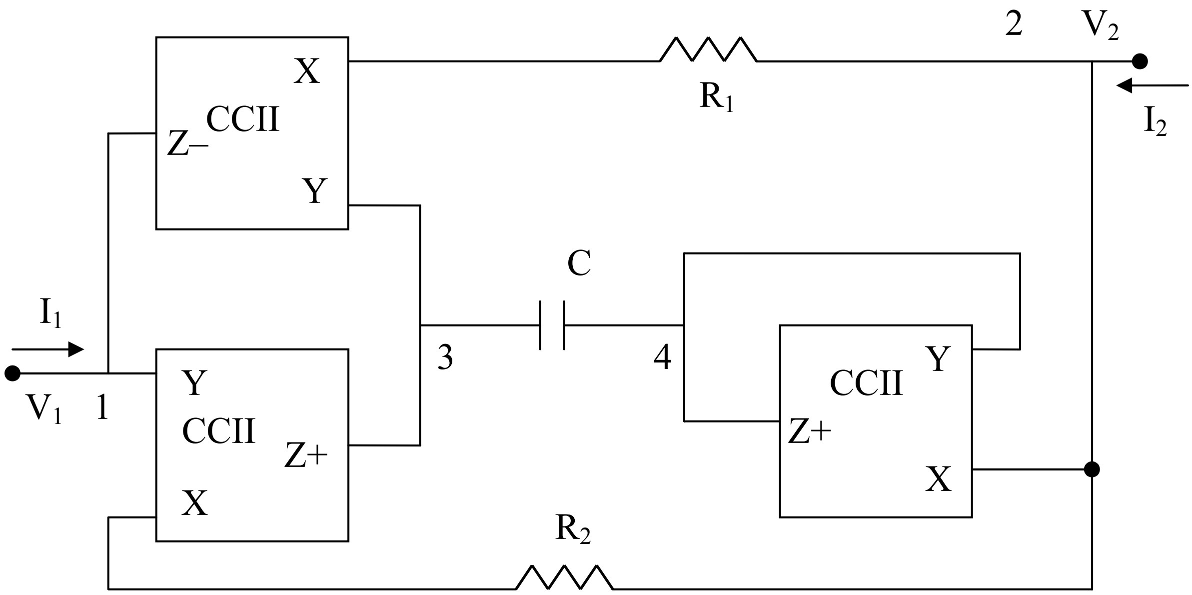


Figure 7(a) A floating inductor using two CCII+ and one CCII– [20]

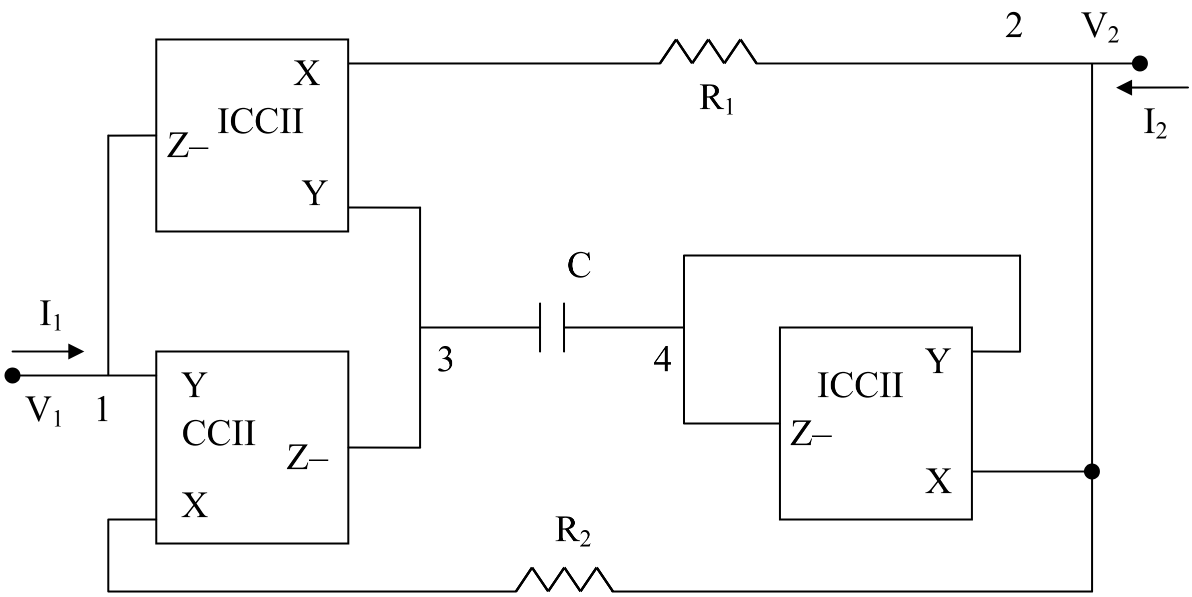


Figure 7(b) A new floating inductor using two ICCII– and one CCII–

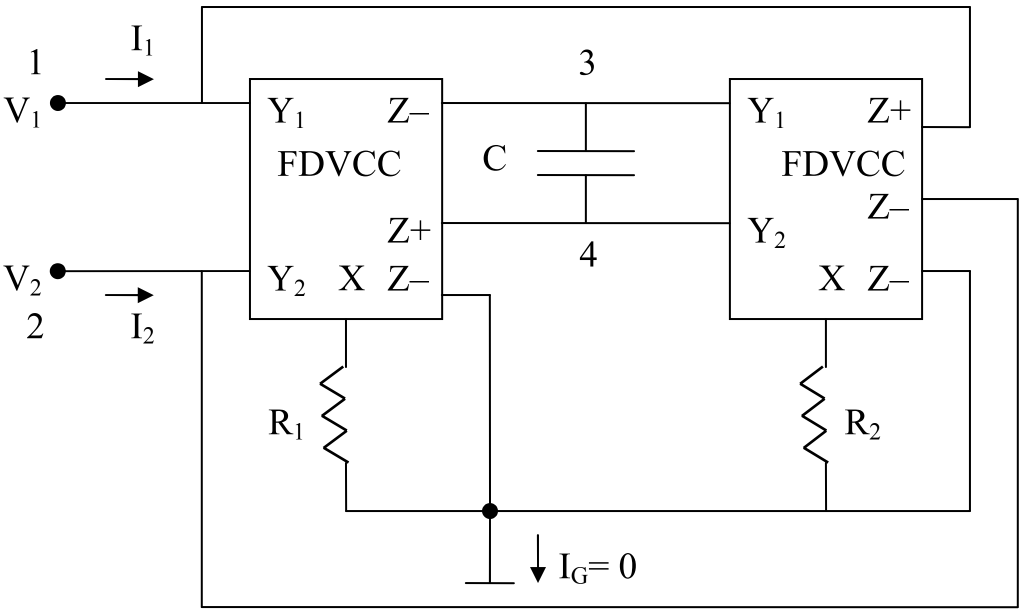


Figure 8(a) A modified floating inductor using two DVCC [21].

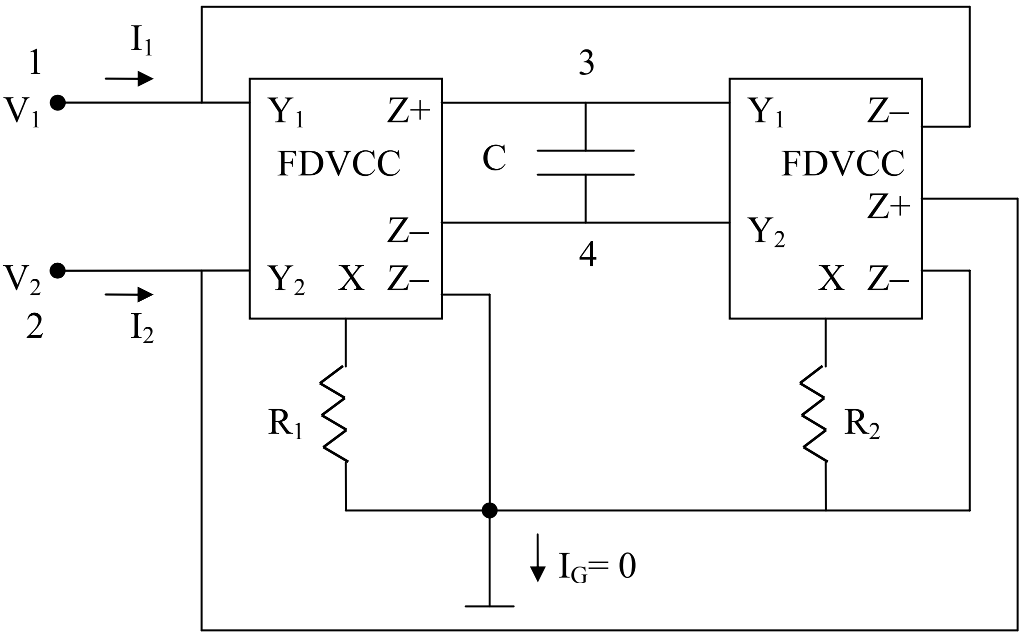


Figure 8(b) Alternative modified floating inductor using two DVCC

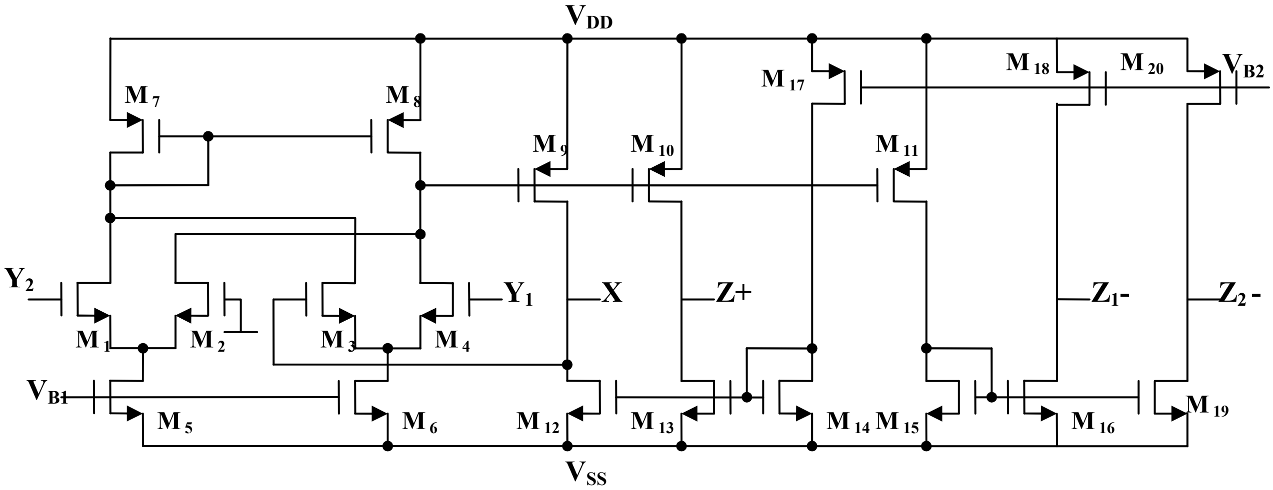


Figure 9 CMOS circuit of the floating DVCC [21]

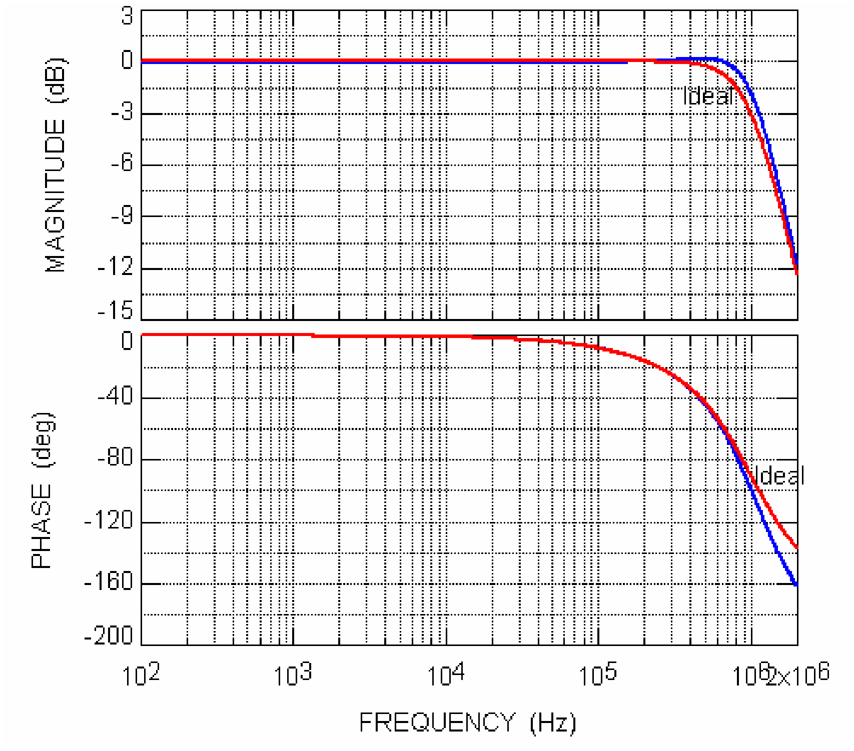


Figure 10(a) Simulation results of a lowpass filter using L of Figure 2

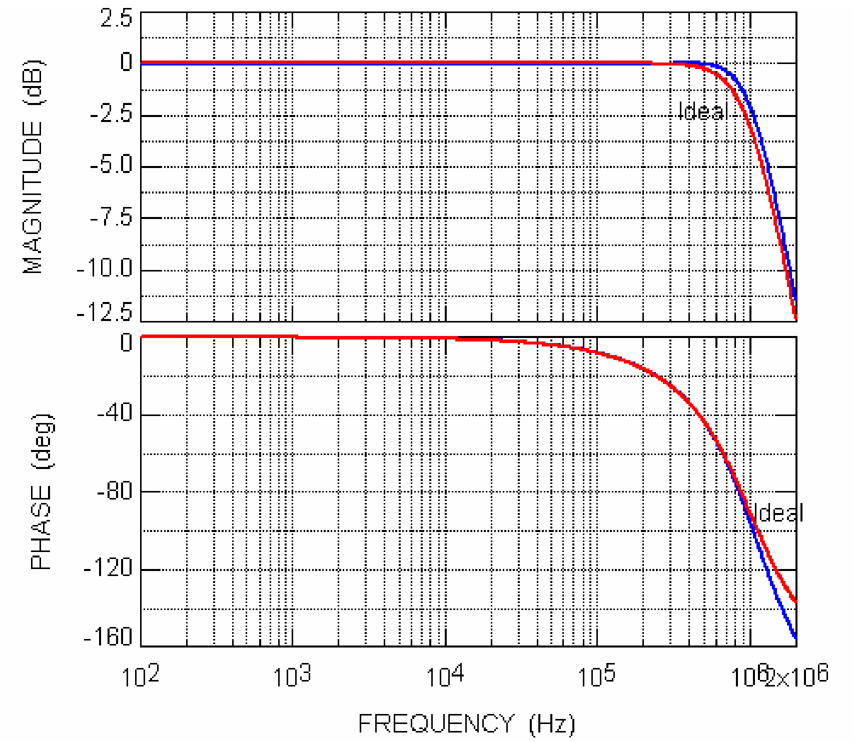


Fig 10(b) Simulation results of a lowpass filter using L of Figure 3(a)

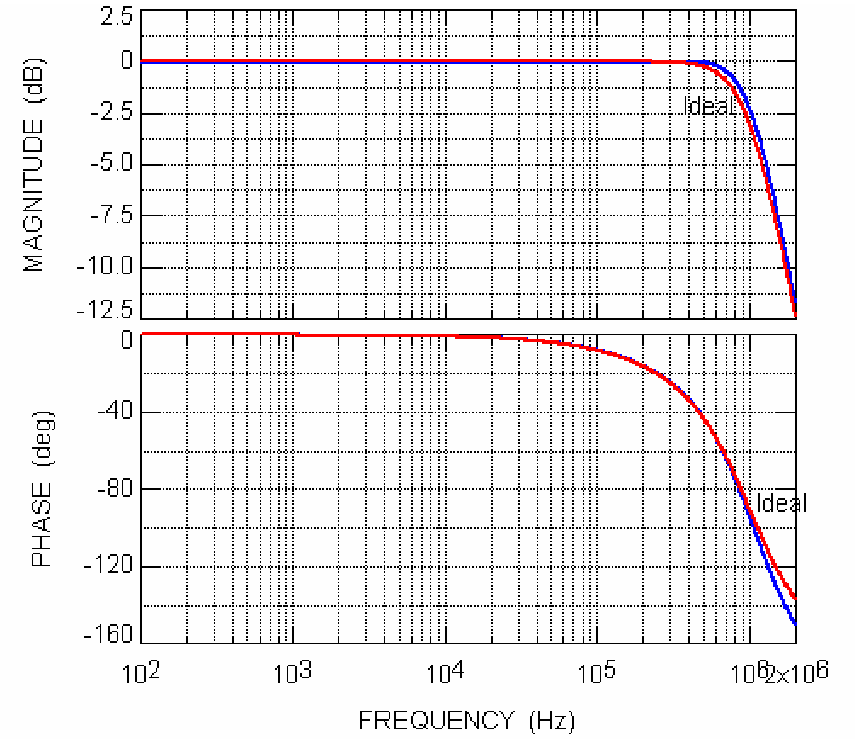


Fig 10(c) Simulation results of a lowpass filter using L of Figure 5

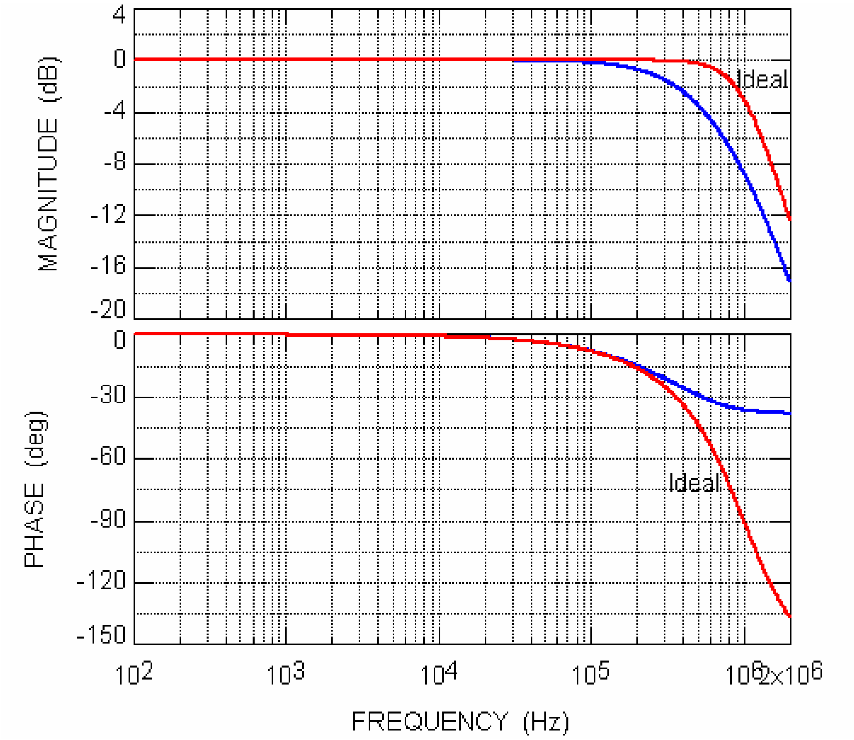


Fig 11(a) Simulation results of a lowpass filter using L of Figure 6(b)

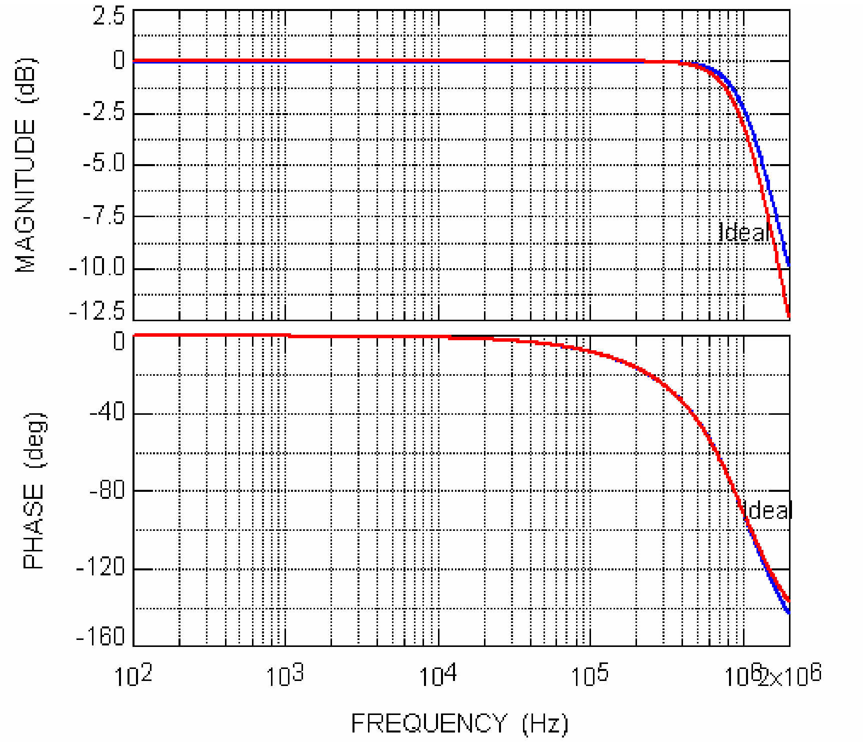


Fig 11(b) Simulation results of a lowpass filter using L of Figure 7(b)

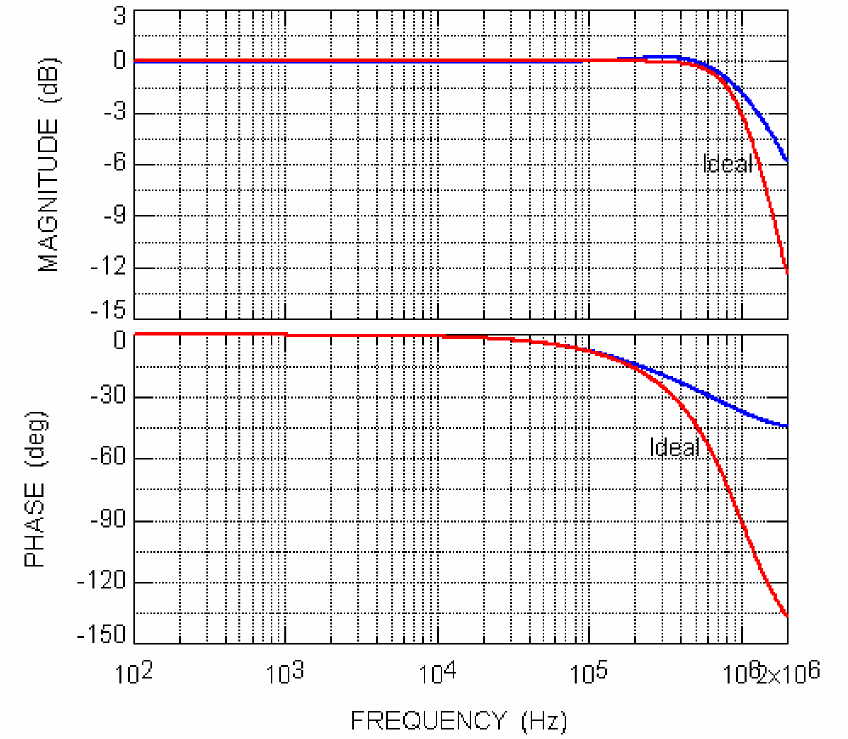


Fig 11(c) Simulation results of a lowpass filter using L of Figure 8(b)